Application Report
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Comparing Bus Solutions

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High-Performance Linear/Interface

ABSTRACT

The strong interest in this application report leads us to publish a second edition. In addition to changes and updates made throughout all sections, new parts have been added, such as M−LVDS, CAN, Clock Interfacing, and VME.

This report is intended to be a reference tool for finding the most appropriate bus interface solution for today's advanced system architectures. It focuses on bus interface solutions for different transmission concepts, and gives an overview of the different bus solutions available from Texas Instruments.

Today, advanced bus system designers have a dilemma: many different solutions can be used to solve the same problem. The task for the designer is to figure out the optimum solution for their special application. In order to ease this choice, this application report has been created. The key bus interface characteristics are presented in a way that developers may easily find the optimum bus solution for their systems.

The report is organized into product family sections to allow easy distinction among various solutions. Each family section of this report covers details on the electrical parameters and appropriate protocols, as well as application and feature-benefit information on the chosen product family. All sections are set up in the same order to aid comparison.

Keywords: ABT, ABTE, AHC, ALVT, BTL, CAN (ISO-11898) , CDC, CompactPCI™, FB+, Firewire, FlatLink™, Gigabit Ethernet/10G Ethernet, GTL, GTLP, HSTL, IEEE1284, IEEE1394, LVDM, LVDS, LVT, M-LVDS, PCI, TIA/EIA-232, RS-232, TIA/EIA-422, RS-422, TIA/EIA-485, RS-485, TIA/EIA-644, TIA/EIA-899, SONET, SSTL, USB, VME, TMS320™ DSP Family.

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1 Overview

In today's information-hungry society, transmitting data over several inches between computer memory and display screen is just as critical as sending it halfway around the globe. Over the past three decades, Texas Instruments has combined its expertise in high-speed digital and analog technologies to address these needs. TI is constantly pushing the capabilities and extending the performance parameters of practically every data transmission standard.

This application report provides the reader with an overview of the different wired bus systems and should give enough insight into which standard or which bus configuration would suit the reader's needs. Before we discuss each standard, its technical features, and the products that TI offers, it is important to understand the fundamentals behind the different bus configurations available.

Data transmission, as the name suggests, is a means of moving data from one location to another. Several important parameters define how the information is transferred. Two of these are the distance, i.e. the space between the sending and the receiving systems and speed, i.e. the rate at which data has to be passed to the receiving device. Different transmission standards, such as TIA/EIA−232, IEEE 1394 and LVDS, provide solutions for various needs in terms of speed and line length as defined by Figure 1.

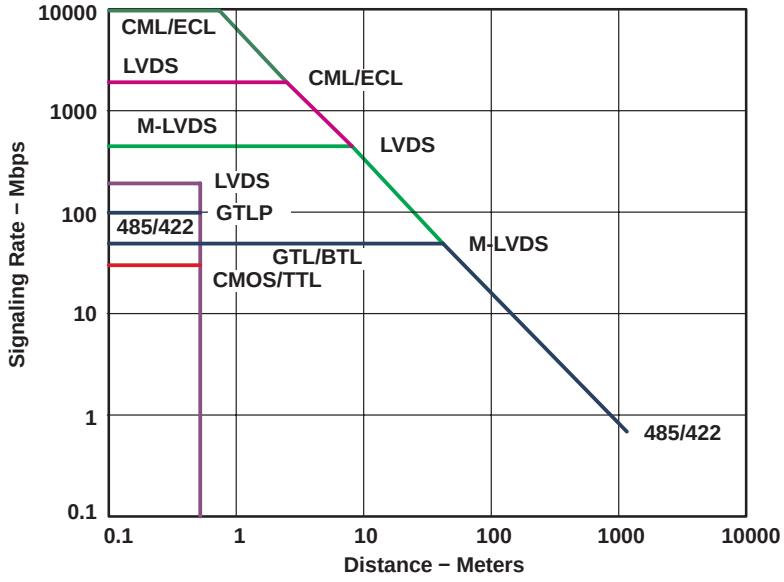


Figure 1. Signaling Rate Versus Cable Length

It can be seen from Figure 1, that as the cable length increases, the speed at which the information is transmitted must be lowered in order to keep the bit-error rate down. Therefore, it is very important to choose the correct standard covering the required communication distance and the needed data rate. Once the choice of standard has been made, the selection of the device required for the specific application can begin. This is certainly not an easy task.

The matrix on the following page has been generated to give a more accurate overview of the different kind of transmission types, the modes, standards, distances, data rates, its benefits, and which TI family would suit which purpose. For every family, Texas Instruments has created a section within this application report describing the characteristics of the standard, and whether or not there is a software overhead. There is, of course, also a family-dedicated web page, containing further information on product data sheets, additional application reports, and the possibility of sampling devices via the Internet. More information is available at TI's web page: http://interface.ti.com.

Table 1. Bus Interface Selection Guide

TYPE	TRANSMISSION MODE	DATA RATE PER LINE	DATA RATE PER DEVICE	DISTANCE	STANDARD	PRODUCT FAMILY
Serial	Multipoint (Multiplex)	25 or 50 Mbps		1.5 m	IEEE1394–1995	IEEE1394 Backplane
		100 − 400 Mbps 800 Mbps		4.5 m several 100 m	IEEE1394–1995 IEEE1394a–2000 IEEE1394b–2002	IEEE1394 Cable IEEE1394 … (PMD ext.)
		12 Mbps		5 m	USB 1.1	USB
		1 Mbps		40 m	CAN (ISO 11898)	HVD / CAN
		35 Mbps		10 m (1200 m)	TIA/EIA 485 (ISO8482)	TIAEIA 485
		400 Mbps		0.5 m (~ 30 m)	TI proprietary	LVDM
		500 Mbps		0.5 m (~ 30 m)	TIA/EIA−899	M−LVDS
	Multidrop (Distributed Simplex)	10 MBps		10 m (1200 m)	TIA/EIA 422 (ITU–T V.11)	TIA/EIA–422
		400/100 Mbps	4 ch: 800/ 400 Mbps	0.5 m (~ 30 m)	TIA/EIA–644 (LVDS) TI proprietary TIA/EIA−899 (M−LVDS)	LVDS/LVDM/M−LVDS
	Point–to–point (Simplex)	512 Kbps		20 m	TIA/EIA–232 (ITU–T V.28)	TIA/EIA–232
		2 Gbps	4 ch: 1600/ 800 Mbps	1 m (~ 30 m)	TIA/EIA–644 (LVDS)	LVDS
Parallel–to–serial Serial–to–parallel	Point–to–point (Simplex)	455 Mbps	4 ch: 1.83 Gbps	< 15 m	TIA/EIA–644 (LVDS)	LVDS SerDes/FlatLink
		1.25 Gbps	1.25 Gpbs full duplex	< 10 m	IEEE P802.3z	Gigabit Ethernet
		2.5 Gbps	4 ch: 10.0 Gbps full duplex	< 10 m	IEEE P802.3ae	10 Gigabit Ethernet
		2.5 Gbps	2.5 Gbps full duplex	< 10 m		Serial Gigabit CMOS
		2.5 Gbps	4 ch: 10.0 Gbps full duplex	< 10 m	i.e. OIF−VSR4−03.0	SONET/SDH
Parallel	Multipoint (Multiplex)	35 Mbps		10 m (1200 m)	TIA/EIA–485 (ISO8482)	TIA/EIA–485
		500 Mbps		0.5 m (~ 30 m)	TIA/EIA−899	M−LVDS
		400/100 Mbps		0.5 m (~ 30 m)	TI proprietary	LVDM
		33/66 MHz		0.2 m	PCI Compact	PCI
		33/66 MHz		0.2 m	PCI	PCI
		4 MHz CLK	16 ch: 64 Mbps	10 m	IEEE Std 1284–1994	AC1284, LVC161284, LV161284
		20 MHz CLK	32 ch: 640 Mbps	0.5 m	CMOS, JESD20, TTL IEEE 1014–1987	AC, AHC, ABT
		33 MHz CLK	20 ch: 660 Mbps	0.5 m	LVTTL as stated in JEDS8–A, June 1994, IEEE 1014–1987	LVTH, ALVT
		40 MHz CLK	16 ch: 640 Mbps	0.5 m	VME64 Standard ANSI/VITA1–1991	ABTE
		60 MHz CLK	16 ch: 960 Mbps	0.5 m	IEEE Std 1194.1–1991	BTL/FB+
		60 MHz CLK	18 ch: 1.08 Gbps	0.5 m	JESD8–3	GTL/GTL+
		100 MHz CLK	18 ch: 1.8 Gbps	0.5 m	JESD8–3	GTLP
		200 MHz CLK	18 ch: 3.6 Gbps	0.1 m	EIA/JESD8–8, EIA/JESD8–9	SSTL

2 Single-Ended Versus Differential Data Transmission

There are currently two forms of operation for electrical interface circuits, single-ended (or unbalanced) and differential (or balanced) data transmission. The difference between single-ended and differential transmission is described below.

2.1 Single-Ended Transmission

Single-ended transmission is performed on one signal line, and the logical state is interpreted with respect to ground. For simple, low-speed interfaces, a common ground return path is sufficient; for more advanced interfaces featuring higher speeds and heavier loads, a single return path for each signaling line (twisted pair cable) is recommended. Figure 2 shows the electrical schematic diagram of a single-ended transmission system.

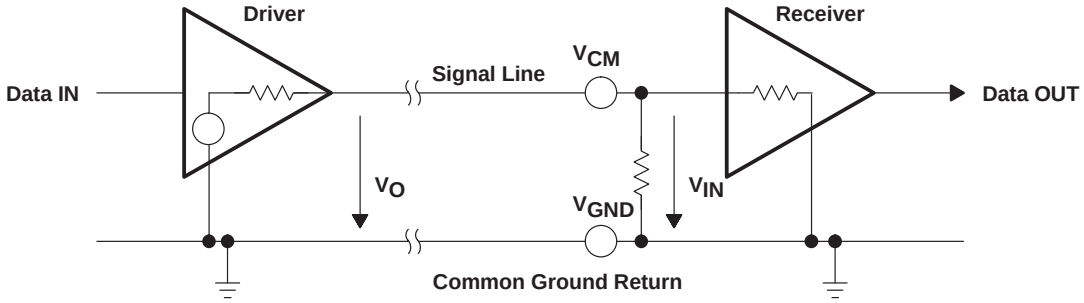


Figure 2. Single-Ended Transmission with Parallel Termination at Line End

2.1.1 Advantages of Single-Ended Transmission

The advantages of single-ended transmissions are simplicity and low cost of implementation. A single-ended system requires only one line per signal. It is therefore ideal for cabling, and when connector costs are more important than the data transfer rate, e.g. PC, parallel printer port or serial communication with many handshaking lines, e.g. EIA-232. Cabling costs can be kept to a minimum with short distance communication, depending on data throughput, requiring no more than a low cost ribbon cable. For longer distances and/or noisy environments, shielding and additional ground lines are essential. Twisted-pair cables are recommended for line lengths of more than 1 meter. The additional efforts might outweigh the previously described cost-advantages.

2.1.2 Disadvantages of Single-Ended Transmission

The main disadvantage of the single-ended solution is its poor noise immunity. Because the ground wire forms part of the system, transient voltages or shifts in voltage potential may be induced (from nearby high frequency logic or high current power circuits), leading to signal degradation. This may lead to false receiver triggering. For example, a shift in the ground potential at the receiver end of the system can lead to an apparent change in the signal, sufficient to drive the input across the thresholds of the receiver, thus increasing its susceptibility to electromagnetic fields.

Crosstalk is also a major concern especially at high frequencies. Crosstalk is generated from both capacitive and inductive coupling between signal lines. Capacitive coupling tends to be more severe at higher signal frequencies as capacitive reactance decreases. The impedance and termination of the coupled line determines whether the electric or the magnetic coupling is dominant. If the impedance of the line is high, the capacitive pickup is large. Alternatively, if the line impedance is low, the series impedance as seen by the induced voltage is low, allowing large induced currents to flow. Single-ended transmission is much more susceptible to external noise and the radiation of EMI is increased compared to differential systems.

In addition to above described noise sources, line reflections have to be considered as well. This is not only important for long transmission lines, short line lengths show critical over- and under-shoot on non terminated lines as well. The higher the speed and the faster the rising and falling edges of the output signal are, the more critical is the line length and even lengths of some centimeters might need to be terminated.

These problems will normally limit the distance and speed of reliable operation for a single-ended link.

2.2 Differential Transmission

For balanced or differential transmission, a pair of signal lines is necessary for each channel. On one line, a true signal is transmitted, while on the second one, the inverted signal is transmitted. The receiver detects voltage difference between the inputs and switches the output depending on which of the two input lines of a channel is more positive. As shown in Figure 3, a signal return path is required.

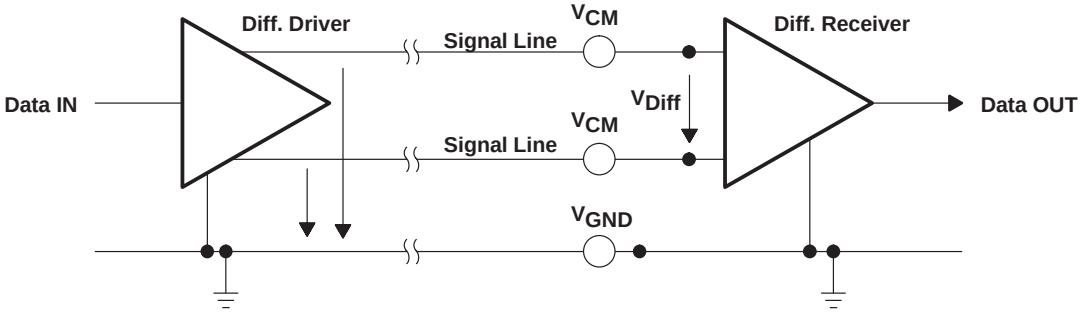


Figure 3. Differential Transmission

Balanced interface circuits consist of a generator with differential outputs and a receiver with differential inputs. Better noise performance stems from the fact that noise is coupled into both wires of the signal pair in the same way and is common to both signals. Due to the common-mode rejection capability of a differential amplifier, this noise is rejected. Additionally, since one signal line emits the opposite signal of the other, the emissions cancel each other. This is true in any case for crosstalk from and to neighboring signal lines.

The twisted-pair cable used in these interfaces, in combination with a correct line termination to avoid line reflections, allows very high data rates. Signaling rates of up to 10 Gbs are possible with differential signaling.

2.2.1 Advantages of Differential Transmission

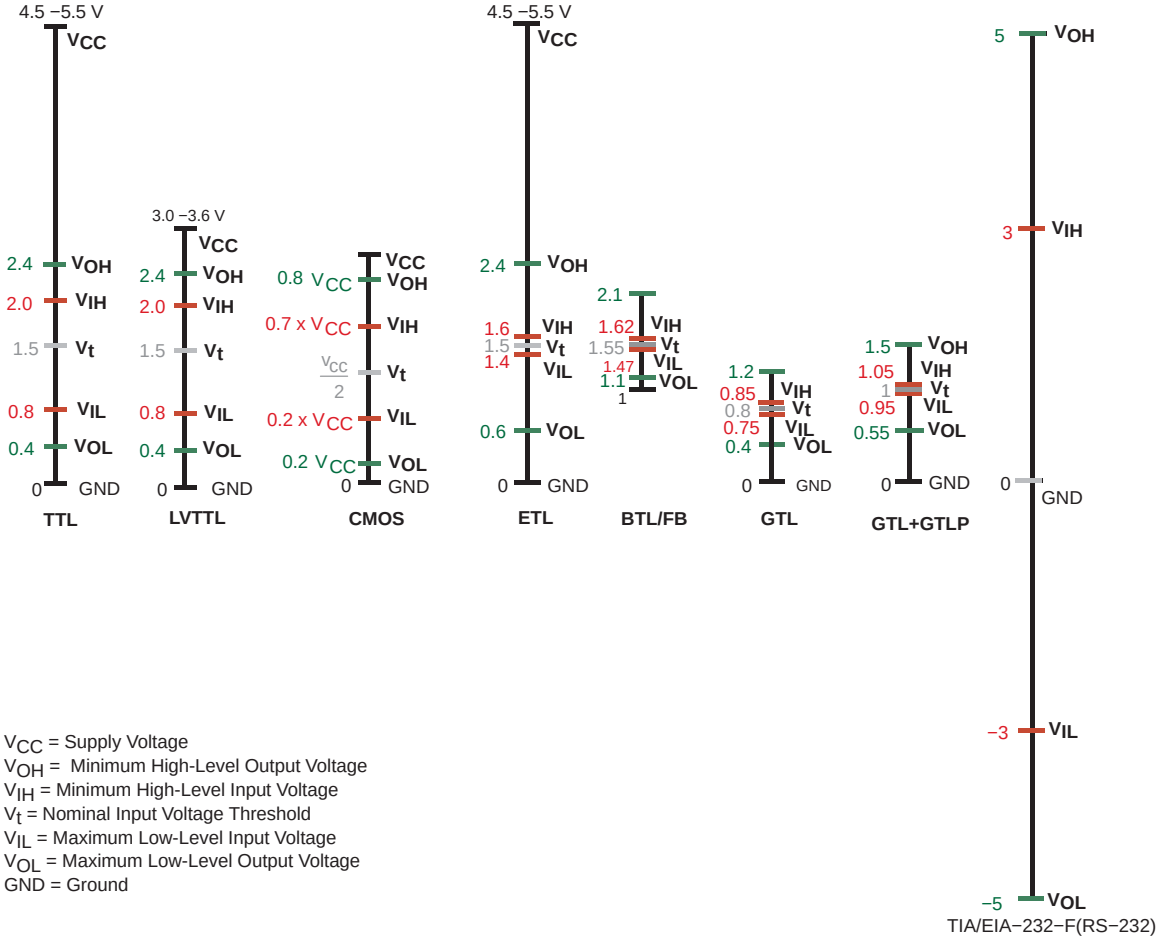
Differential data transmission schemes are less susceptible to common-mode noise than single-ended schemes. Because this kind of transmission uses two wires with opposite current and voltage swings compared to only one wire for single-ended, any external noise is coupled onto the two wires as a common mode voltage and is rejected by the receivers. This two-wire approach with opposite current and voltage swings also radiates less electro-magnetic interference (EMI) noise than single-ended signals due to the canceling of magnetic fields.

2.2.2 Disadvantages of Differential Transmission

Cost is the primary disadvantage of differential transmission. However, efforts have been made to reduce the costs of these complex devices by developing them in a CMOS process, or to improve performance by using LinBiCMOS processes for example, for LVDS further information on process technologies can be found at http://www−s.ti.com/sc/psheets/slla065/slla065.pdf. Furthermore, the high data-rates that are possible with differential transmission require very well-defined line impedance and correct line termination to avoid line reflections. For this method of transmission twisted pair cables instead of less expensive multi–conductor cables are recommended.

3 Standard Switching Levels

All standards are defined through input and output switching levels. Some of these levels are defined by the Joint Electronic Device Engineering Council, otherwise known as JEDEC, and others are specified in the corresponding standard. Figure 4 shows the single-ended switching levels.



V_{CC} = Supply Voltage
V_{OH} = Minimum High-Level Output Voltage
V_{IH} = Minimum High-Level Input Voltage
V_t = Nominal Input Voltage Threshold
V_{IL} = Maximum Low-Level Input Voltage
V_{OL} = Maximum Low-Level Output Voltage
GND = Ground

Figure 4. Switching Levels of Single-Ended Transmission Standards

4 Connectivity

When designing a data transmission system, bus-system designers have numerous ways of connecting the transmitters, receivers, boards, backplanes and racks. Figure 5 shows how, in a typical backplane rack, the cards can be linked up. The backplane itself consists of a parallel bus type configuration with each card slotted onto that bus via a connector. In some situations, it is necessary to connect either individual cards together, or a backplane to a card, etc. It would be very inconvenient to connect these devices together via a parallel cable. Serial techniques supporting a very high data rate cope with this kind of need.

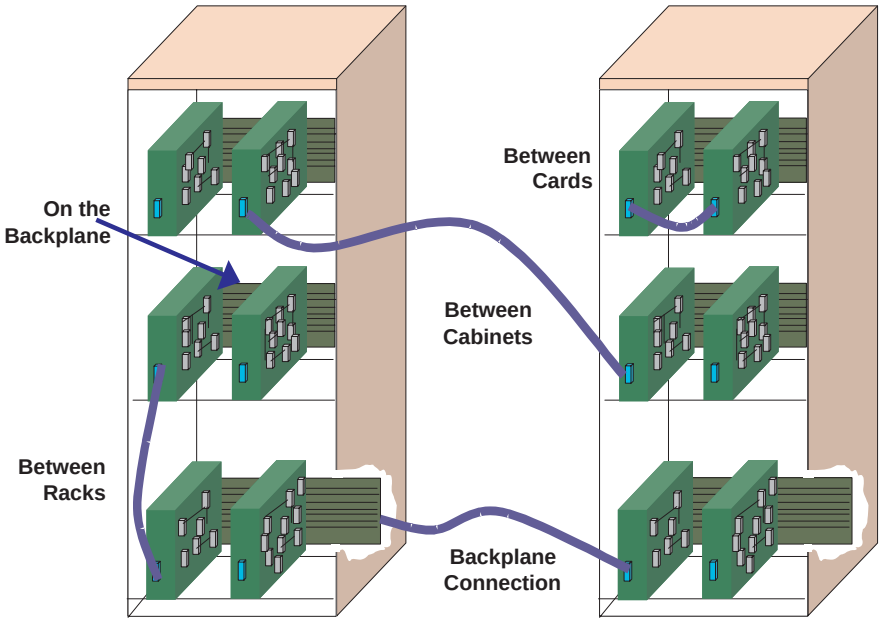


Figure 5. Different Interconnection Scenarios

LVDS and IEEE1394b are two of the latest standards that have been developed for high-speed point–to–point serial transmission. What are the benefits of serial transmission compared to parallel transmission? The next section explains the principle behind the two different techniques and outlines the benefits and shortcomings of both of them.

5 Parallel Versus Serial Transmission

Figure 6 illustrates the difference between parallel and serial transmission. In a purely parallel situation, the driver attached to the bus places n-bits of data onto it and all the information is sent at the same time along the backplane.

In the case of serial transmission, the data must first be converted to a serial stream. This is called the serialization. The serial data is then transmitted at high speed along the line to the receiver, which must then deserialize the information back into the original parallel data. In order for the serial technique to achieve the same data rates as the parallel one, the data must be sent along the line at a much higher speed than on the parallel bus. Both methods have their advantages and disadvantages.

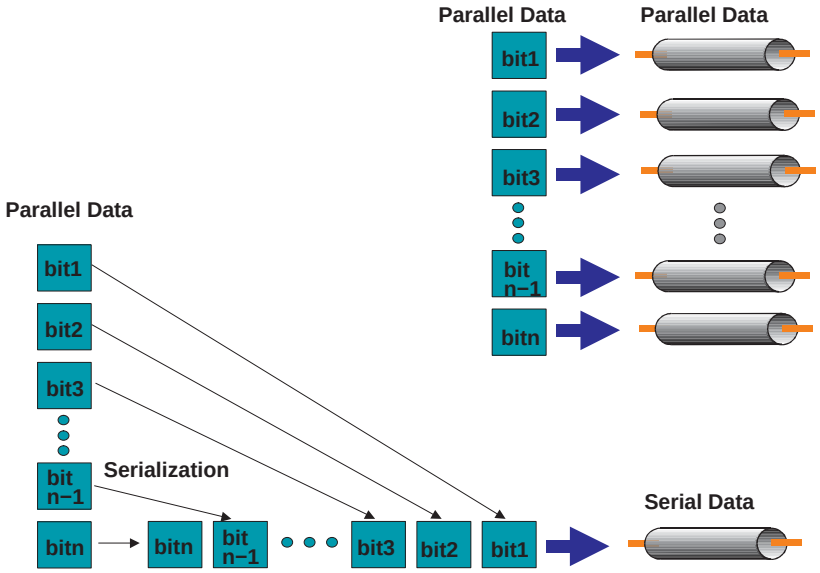


Figure 6. Principle of Parallel and Serial Transmission

5.1 Advantages of Parallel Transmission

- Parallel buses do not have the time delay required by serial buses to accumulate and decode a whole bock of data. Single lines can be configured for controlling purposes, potentially enabling a faster throughput.
- Many industrial and telecom applications already use parallel backplanes. This means that many designers and engineers are familiar with these kinds of systems and have the knowledge and the experience to quickly implement them.

5.2 Disadvantages of Parallel Transmission

- A disadvantage of parallel data bus structure is the larger number of conductors and the space needed to connect them. This results in more cost.
- The ultimate transfer rate of a parallel bus is limited by the time difference between the different signal paths.

5.3 Advantages of Serial Transmission

- No line-to-line timing skew
- Serial data uses fewer wires and lowers cable and connector costs and size.
- Savings on board space, and power consumption per bit

5.4 Disadvantages of Serial Transmission

- Serial links are generally limited to point-to-point connections.
- There is overhead above the actual data payload that uses transmission bandwidth.
- Higher signaling rates shorten the transmission distance.

6 Data Transmission Topologies

This section briefly explains the Point-to-Point, Multidrop and Multipoint topologies. Figures show the single-ended and differential solutions for each topology.

6.1 Point-to-Point (Simplex)

This configuration is implemented with one transmitter and one receiver per line. Transmission is possible only in one direction, i.e. unidirectional.

Figure 7. Point-to-Point Connection

6.2 Multidrop (Distributed Simplex)

A point-to-point configuration is implemented with one transmitter and many receivers per line (Figure 8). Only unidirectional transfer is possible.

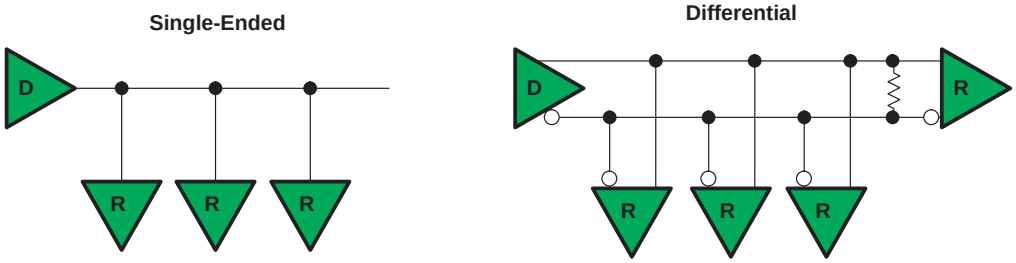


Figure 8. Multidrop Connection

6.3 Multipoint (Multiplex)

This configuration is implemented with many transmitters and many receivers per line, shown in Figure 9. In practice, this solution is normally realized with a transmitter-receiver pair called a transceiver. Not all of the participants have to be transceivers. Any combination of receivers, transmitters and transceivers, is possible for this topology. Transmission is possible in either direction, i.e. bidirectional.

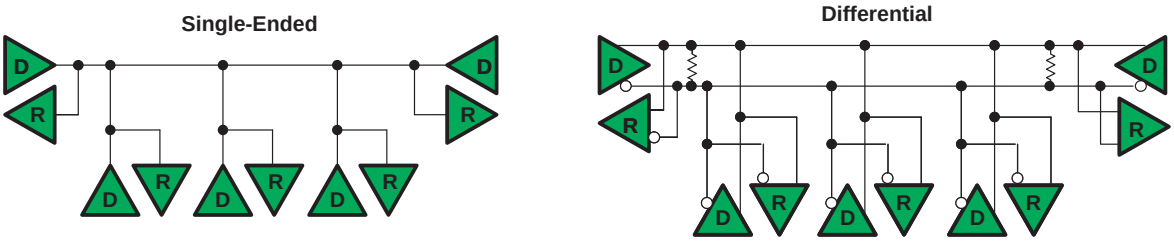


Figure 9. Multipoint Connection Using Multiple Transceivers

7 IEEE 1394 Cable and Backplane Applications (FireWire)

IEEE designations for a high performance serial bus are the 1394-1995,1394a-2000 and 1394b-2002. This serial bus defines both a backplane (for example, VME, FB+) physical layer and a point-to-point cable-connected virtual bus. The backplane version operates at 12.5, 25, 50 or 100 Mbps, whereas the cable version supports data rates of 100, 200, and 400 Mbps in 1394a-2000, 800 Mbps and 1600 Mbps in 1394b. All versions are compatible at the link layer and above. The interface standard defines the transmission method, media in the cable version, and protocol.

The primary application of the cable version is the interconnection of digital A/V equipment and integration of I/O connectivity at the back panel of personal computers using a low-cost, scalable, high-speed serial interface. The 1394 standard also provides new services such as real-time I/O, and live connect/disconnect capability for external devices. Furthermore, it can be used in automotive, industrial, instrumentation, and medical applications (such as motor control, surveillance and medical monitoring, etc.)

7.1 Electrical

The 1394 standard is a packet-transaction-based technology for cable- or backplane-based environments. Both chassis and peripheral devices can use this technology. The 1394 serial bus is organized as if it were memory space interconnected between devices, or as if devices resided in slots on the main backplane. Device addressing is 64 bits wide, partitioned as 10 bits for bus ID, 6 bits for node ID and 48 bits for memory addresses. The result is the capability to address up to 1023 buses, with each having up to 63 nodes, each with 281 terabytes of memory. Memory–based addressing, rather than channel addressing, views resources as registers or memory that can be accessed with processor-to-memory transactions. Each bus entity is termed a unit, to be individually addressed, reset, and identified. Multiple nodes may physically reside in a single module, and multiple ports may reside in a single node.

Some key features of the 1394 topology are multi-master capabilities, live connect/disconnect (hot plugging) capability, genderless cabling connectors on interconnect cabling, and dynamic node address allocation as nodes are added to the bus. Another feature is that transmission speed is scalable from approximately 100 Mbps to 800 Mbps. Future devices shall support as well 1.6 Gbps and 3.2 Gbps.

Nodes may act as a repeater, allowing nodes to be chained together to form a relatively unrestricted topology. 1394-1995 and 1394a-2000 based cable PHYs (physical layer devices) use cables with power wires. Equipment/devices meeting the 1394 standard that are not switched on can still power their PHYs from the 1394-bus, thus acting as a repeater or hub. Equipment with low power consumption can be powered directly from the 1394 bus. By using the maximum number of 16 hops (1394a-2000 allows 24 hops) with regular 4.5-m cables, the maximum end-to-end distance of 72 m is reached. 1394b-2002 defines new transmission media and modulation types. Data can now be transmitted over several types of optical cables and low cost twisted pair cables. Heterogeneous networks allow optimum solutions in terms of cost (use electrical cable where possible; use optical cables where needed). While remote powering across optical cable sections is no longer possible with 1394b, you may ask if this standard extension is still backward compatible to 1394-1995. Well, you cannot connect an optical cable with an electrical outlet. In such configurations you need a simple cable converter. Bilingual PHYs like the TSB81BA3 are used as translators between the 1394-1995 and 1394a-2000 world (that use DS coding) and the 1394b world (that use 8B10B coding).

DS coding in 1394-1995 and 1394a is a method that uses common mode DC signals for arbitration and speed signaling. An encoded clock that can easy be recovered simplifies fast detection of data with different speeds.

8B10B coding in 1394b allows DC-free data transmission which is needed when transformers or capacitors (to separate ground domains) are used in the signal path. The bit representation is the same for electrical or optical, it just needs an optical transceiver to go optical (LED driver and LED on TX, photodiode and sense amplifier on RX).

It's simple! if you can connect it with cables, it is compatible back and forth (from 100 Mbps to 3.2 Gbps).

Table 2. 1394 PMD Connection Matrix

Speed	Reach	100DS	200DS	400DS	100	200	400	800	1600
STP (1394cbl)	4.5m	1394-1995	1394-1995	1394-1995			1394b	1394b	1394b
UTP−5	100m				1394b				
POF	50m				1394b	1394b			
HPCF	100m				1394b	1394b			
MMF	100m						1394b	1394b	1394b
Remote-Power	na	yes	yes	yes			on STP	on STP	on STP

7.2 Protocol

Both asynchronous and isochronous data transfers are supported. The asynchronous format transfers data and transaction layer information to an explicit address. The isochronous format broadcasts data based on channel numbers rather than specific addressing. Isochronous packets are issued on the average of each 125 μs in support of time-sensitive applications. Providing both asynchronous and isochronous formats on the same interface allows both non-real-time and real-time critical applications on the same bus.

The cable environment's tree topology is resolved during a sequence of events triggered each time a new node is added or removed from the network. This sequence starts with a bus reset phase, where previous information about a topology is cleared. The tree ID sequence determines the actual tree structure, and a root node is dynamically assigned, or it is possible to force a particular node to become the root. After the tree is formed, a self-ID phase allows each node on the network to identify itself to all other nodes. During the self-ID process, each node is assigned an address. After all of the information has been gathered on each node, the bus goes into an idle state waiting for the beginning of the standard arbitration process.

An additional feature is the ability of transactions at different speeds to occur on a single device medium (for example, some devices can communicate at 100 Mbps while others communicate at 200 Mbps, 400 Mbps or 800Mbps). Use of multispeed transactions on a single 1394 serial bus requires consideration of each node's maximum capabilities when laying out the connections to ensure that the path between two higher–speed nodes is not restricted by a device with lower–rate capabilities.

The backplane physical layer shares some commonality with the cable physical layer. Common functions include: bus state determination, bus access protocols, encoding and decoding functions, and synchronization of received data to a local clock.

7.3 Applicability and Typical Application for IEEE 1394

The transmission of data without burdening the host unit creates a huge market for IEEE1394. Not only does the computer-based equipment in private households require an interface solution for the home and home office network, but also the evolving markets of digital broadcasts, interactive services, games, and home shopping requires a high speed network. The introduction of digital set top boxes, which enable the reception of these services, enables the capability to transmit digital data not only to consumer devices like digital TV, but also to PC and storage media. In addition to the consumer, PC, and PC-peripheral markets, many industrial applications can be covered by IEEE1394.

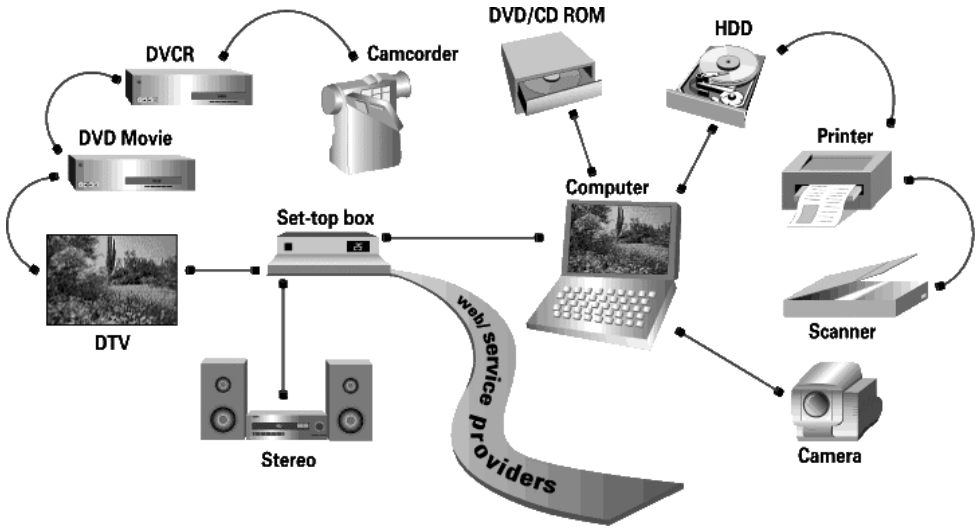


Figure 10. Possible Interconnections Using 1394 as Interface

7.4 Applicability and Typical Application for IEEE 1394 Backplane

The 1394 backplane serial bus (BPSB) plays a supportive role in backplane systems, specifically GTLP, FutureBus+™, VME64, and proprietary backplane bus systems. This supportive role can be grouped into three categories:

- Diagnostics: Alternate control path to the parallel backplane bus; test, maintenance, and troubleshooting; software debug and support interface.
- System enhancement: Fault tolerance; live insertion; CSR access; auxiliary bus to the parallel backplane bus
- Peripheral monitoring: Monitoring of peripherals (disk drives, fans, power supplies, etc.) in conjunction with 1394 cable serial bus.

FutureBus+ is a trademark of IEEE, Inc.

The TSB14AA1 and SN74GTLP1394 provide a way to add high-speed 1394 connections to almost any backplane.

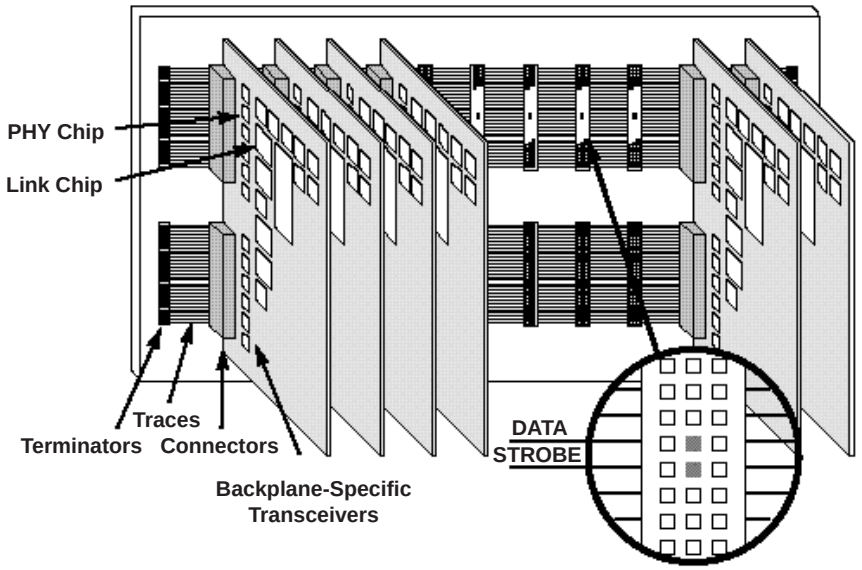


Figure 11. Principle Application Setup Using 1394 Interface

7.5 Features

- Real-time data transfer for multimedia applications
- 100, 200, and 400 Mbps data rates for high-speed applications in cable environments at 1394.a (2000) and 800 Mbps data rates at 1394.b
- 25 and 50 Mbps data rates for backplane environments
- Live connection/disconnection without data loss or interruption
- Automatic configuration supporting plug and play
- Free network topology allowing branching and daisy-chaining
- Assured bandwidth assignments for real-time applications

Table 3. Top IEEE 1394 Link Layer Device List (PC)

DEVICE	SPEED	POWER	PACKAGE
TSB12LV26	400 Mbps	3.3 V (5-V tolerance)	100-pin TQFP
TSB12LV21B	400 Mbps	3.3 V (5-V tolerance)	176-pin TQFP
TSB15LV01	400 Mbps	3.3 V (5-V tolerance)	80-pin TQFP
TSB42AA9A	400 Mbps	3.3 V (5-V tolerance)	100-pin TQFP
TSB82AA2	800 Mbps	3.3 V	144-pin LQFP

Table 4. Top IEEE 1394 Integrated Device List (PC)

DEVICE	PORTS	SPEED	POWER	PACKAGE
TSB43AB21A	1	400 Mbps	3.3 V (5-V tolerance)	128-pin TQFP
TSB43AB22A	2	400 Mbps	3.3 V (5-V tolerance)	128-pin TQFP
TSB43AB23	3	400 Mbps	3.3 V (5-V tolerance)	128-pin TQFP

Table 5. Top IEEE 1394 Integrated Device List (Non-PC)

DEVICE	PORTS	SPEED	POWER	PACKAGE
TSB43AA82A	2	400 Mbps	3.3 V (5-V tolerance)	144-pin LQFP
TSB43CA43A	3	400 Mbps	3.3 V (1.8-V core)	176-pin LQFP
TSB43CB43A	3	400 Mbps	3.3 V (1.8-V core)	176-pin LQFP

Table 6. Top IEEE 1394 Link Layer Device List (Non-PC)

DEVICE	SPEED	POWER	PACKAGE
TSB42AA4	400 Mbps	3.3 V (5-V tolerance)	128-pin TQFP
TSB42AB4A	400 Mbps	3.3 V (5-V tolerance)	128-pin TQFP
TSB12LV01B	400 Mbps	3.3 V (5-V tolerance)	100-pin TQFP
TSB12LV32	400 Mbps	3.3-V (5-V tolerance)	100-pin TQFP

Table 7. Top IEEE 1394 Physical Layer Device List

DEVICE	PORTS	SPEED	POWER	PACKAGE
TSB41AB1	1	400 Mbps	3.3 V (5-V tolerance)	48/64-pin TQFP
TSB41AB2	2	400 Mbps	3.3 V (5-V tolerance)	64-pin HTQFP
TSB41AB3	3	400 Mbps	3.3 V (5-V tolerance)	80-pin HTQFP
TSB41LV04A	4	400 Mbps	3.3 V (5-V tolerance)	80-pin HTQFP
TSB41BA3	3	400 Mbps	3.3 V	80-pin TQFP
TSB17BA1	1	n/a	3.3 V	24-pin TSSOP
TSB41LV06	6	400 Mbps	3.3 V (5-V tolerance)	100-pin HTQFP
TSB81BA3	3(bilingual)	800 Mbps	3.3 V (1.8-V core)	80-pin HTQFP
TSB14AA1A (Backplane)	1	100 Mbps	3.3-V	68-pin TQFP
TSB14C01A (Backplane)	1	100 Mbps	5 V	68-pin TQFP

8 Universal Serial Bus (USB)

Flexibility, expandability, and ease of use are all important in meeting the needs of the growing numbers of PC users. Until now, the traditional PC's peripheral expansion capabilities have largely limited these important user concerns. The new USB standard is an important tool that gives a simple way to expand a system in a virtually unlimited number of ways. Most important, this functionality is available today.

USB is designed to simplify a user's effort by combining the PC's many existing interfaces, like the TIA/EIA-232C serial ports, parallel port, game/MIDI port and more, into a single, easy-to-use connector. This capability greatly reduces the complexity of the system and gives manufacturers the ability to develop highly integrated products. The true plug-and-play capability of USB also signals an end to the often complex process of adding system peripherals.

8.1 Electrical

The USB physical interconnect is a tiered-star topology. A hub is at the center of each star. Each wire segment is a point-to-point connection between the host and a hub or function, or a hub connected to another hub or function. The USB transfers signal and power over a four-wire cable. The signaling occurs over two wires on each point-to-point segment.

There are three data rates: full-speed signaling bit rate at 12 Mbps, a limited capability low-speed signaling mode at 1.5 Mbps and high-speed mode at 480 Mbps. All modes can be supported in the same USB bus by automatic dynamic mode switching between transfers. The low-speed mode is defined to support a limited number of low-bandwidth devices, such as a mouse, because more general use would degrade bus utilization. The clock is transmitted, encoded along with the differential data. The clock encoding scheme is NRZI with bit stuffing to ensure adequate transitions. A SYNC field precedes each packet to allow the receiver(s) to synchronize their bit recovery clocks. The cable also carries VBUS and GND wires on each segment to deliver 5 V power to devices.

8.2 Protocol

The USB is a polled bus. The host controller initiates all data transfers.

All bus transactions involve the transmission of up to three packets. Each transaction begins when the host controller, on a scheduled basis, sends a USB packet describing the type and direction of transaction, the USB device address, and endpoint number. This packet is referred to as the token packet. The addressed USB device selects itself by decoding the appropriate address fields. In a given transaction, data is transferred either from the host to a device or from a device to the host. The direction of data transfer is specified in the token packet. The source of the transaction then sends a data packet or indicates it has no data to transfer. The destination, in general, responds with a handshake packet indicating whether the transfer was successful.

The USB data transfer model between a source or destination on the host and an endpoint on a device is referred to as a pipe. There are two types of pipes: stream and message. Stream data has no USB-defined structure, whereas message data does. Additionally, pipes have associations of data bandwidth, transfer service type, and endpoint characteristics like directionality and buffer sizes. Most pipes are created when a USB device is configured. One message pipe, the default control pipe, always exists once a device is powered, in order to provide access to the device configuration, status, and control information.

The transaction schedule allows flow control for some stream pipes. At the hardware level, this prevents buffers from underrun or overrun situations by using a negative acknowledgment handshake to decrease the data rate. When negative acknowledged, a transaction is retried when bus time is available. The flow control mechanism permits the construction of flexible schedules that accommodate concurrent servicing of a heterogeneous mix of stream pipes. Thus, multiple stream pipes can be serviced at different intervals and with packets of different sizes.

8.3 Applicability and Typical Applications

USB is a PC-centric system designed to interconnect up to 127 peripherals to the PC including the ones pictured below: keyboard, mouse, printer, modem, etc. Due to the tiered star topology, a hub is needed at the center of each star.

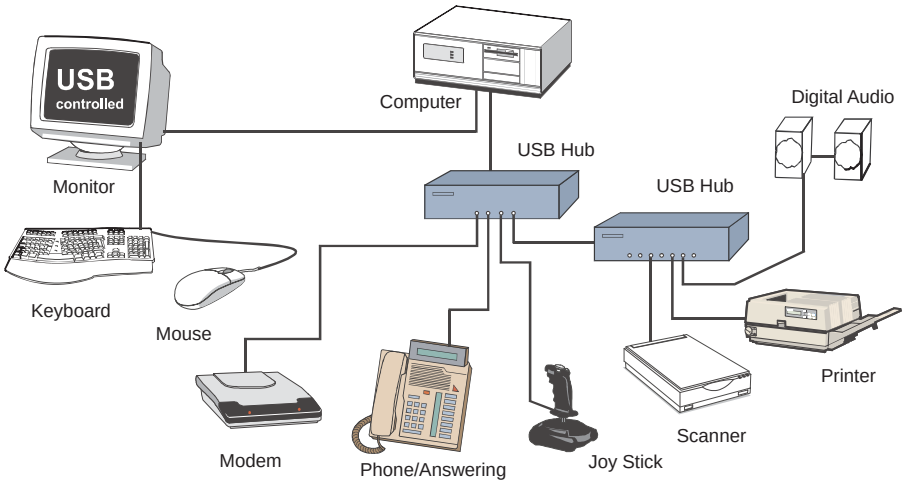


Figure 12. USB - Tiered Star Topology

8.4 Features

- Single PC supports up to 127 devices
- Data rates of 1.5 Mbps,12 Mbps, and 480 Mbps supported
- Ends confusion of multiple add-in cards for ease of use
- Universal connectors and cables for all devices and applications
- Auto configuration upon connection for real plug and play
- Assured bandwidth for real-time applications

Table 8. Top USB Device List

DEVICE	DOWNSTREAM PORTS	Special Feature	POWER	PACKAGE
TUSB2036	2/3	Serial EEPROM IF	3.3 V	32–pin LQFP
TUSB2136	2	Integrated GP controller	3.3 V	64–pin LQFP
TUSB2046B	4	Serial EEPROM IF	3.3 V	32–pin LQFP
TUSB2077A	7	Serial EEPROM IF	3.3 V	48–pin LQFP
TUSB5052	5	USB to 2 serial port	3.3 V	100-pin LQFP
TUSB3210	X	Universal Serial Bus General-Purpose Device Controller	3.3V	64-pin LQFP
TUSB3200 A	X	USB Streaming Controller (STC)	3.3V	52-pin TQFP
TUSB3410	X	RS-232/IrDA serial-to-USB Converter	3.3 V	32-pin LQFP

9 TIA/EIA-232

Usually, it is based on or is identical to other standards, e.g., EIA/TIA-232-F. The following section gives a closer view of these specifications, their benefits, and applicability. Where appropriate, the protocol is briefly described.

TIA/EIA-232, previously known as RS-232 was developed in the 1960's to interconnect layers of the interface (ITU−T V.11), but also the pin-out of the appropriate connectors (25-pin D-type or 9-pin DB9S) (ISO 2210) and the protocol (ISSUED-T V.24). The control lines data carrier detect (DCD), data set ready (DSR), request to send (RTS), clear to send (CTS), data terminal ready (DTR), and the ring indicator (RI) might be used, but do not necessarily have to be (for example, the PC serial mouse utilizes only RI, TD, RD and GND). Although the standard supports only low-speed data rates and line length of approximately 20 m maximum, it is still widely used. This is due to its simplicity and low cost.

9.1 Electrical

TIA/EIA-232 has high signal amplitudes of ± (5 V to 15 V) at the driver output. The triggering of the receiver depends on the sign of the input voltage: that is, it senses whether the input is above 3 V or less than −3 V. The line length is limited by the allowable capacitive load of less than 2500 pF. This results in a line length of approximately 20 m. The maximum slope of the signal is limited to 30 V/µs. The intention here is to limit any reflections that can occur to the rise- and fall-times of the signal. Therefore, transmission line theory does not need to be applied, so no impedance matching and termination measures are necessary. Due to the voltage swings of -5...15 to 5...15 V, a dual supply voltage was necessary in the past. Many devices operate with single supplies, generating the large positive and negative driver output voltage swings with integrated charge-pumps.

9.2 Protocol

Different from other purely electrical-layer standards, TIA/EIA-232 defines not only the physical layer of the interface (ITU-T V.11), but also the pinout of the appropriate connectors (25-pin D-type or 9-pin DB9S) (ISO 2210), and the protocol (ITU-T V.24). The interface standard also specifies handshake and control lines, in addition to the unidirectional receive data line (RD) and the transmit data line (TD).

9.3 Applicability

TIA/EIA–232 is historically associated with computers interfacing with peripherals at low speed, short distance, for example, mouse, modem, joystick, etc., or to interconnect two PCs (that is, null modem, Figure 13). Today other equipment also uses the TIA/EIA-232 I/O. One such example is for programming purposes.

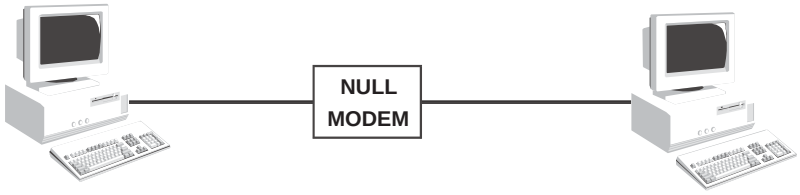


Figure 13. Null Modem Application Using RS232

9.4 Features

- Established standard
- Inexpensive
- Universally used

Table 9. Top TIA/EIA-232 Device List

DEVICE	BIT WIDTH	POWER	ESD PROTECTION	PACKAGE
MAX3221	1 driver/ 1 receiver	V_{CC}: 3.3 V, 5 V I/O: LVTTL/ RS232 250 kbit/s	±15 kV HBM ESD (on bus pins)	16-pin SSOP, TSSOP
MAX3222	2 drivers/ 2 receivers	V_{CC}: 3.3 V, 5 V I/O: LVTTL/ RS232 250 kbit/s	±15 kV HBM ESD (on bus pins)	20-pin SOIC, SSOP, TSSOP
MAX3223	2 drivers/ 2 receivers	V_{CC}: 3.3 V, 5 V I/O: LVTTL/ RS232 250 kbit/s	±15 kV HBM ESD (on bus pins)	20-pin SOIC, SSOP, TSSOP
MAX3232	2 drivers/ 2 receivers	V_{CC}: 3.3 V, 5 V I/O: LVTTL/ RS232 250 kbit/s	±15 kV HBM ESD (on bus pins)	16-pin SOIC, SSOP, TSSOP
MAX3238	5 drivers/ 3 receivers	V_{CC} :3.3 V, 5 V I/O: LVTTL/ RS232 250 kbit/s	±15 kV HBM ESD (on bus pins)	28-pin SSOP, TSSOP
MAX3243	3 drivers/ 5 receivers	V_{CC}: 3.3 V, 5 V I/O: LVTTL/ RS232 250 kbit/s	±15 kV HBM ESD (on bus pins)	28-pin SSOP, TSSOP
SN75C3221	1 driver/ 1 receiver	V_{CC} :3.3 V, 5 V I/O: LVTTL/ RS232 1 Mbit/s	±15 kV HBM ESD (on bus pins)	16-pin SSOP, TSSOP
SN75C3222	2 drivers/ 2 receivers	V_{CC}: 3.3 V, 5 V I/O: LVTTL/ RS232 1 Mbit/s	±15 kV HBM ESD (on bus pins)	20-pin SOIC, SSOP, TSSOP
SN75C3223	2 drivers/ 2 receivers	V_{CC}: 3.3 V, 5 V I/O: LVTTL/ RS232 1Mbit/s	±15 kV HBM ESD (on bus pins)	20-pin SOIC, SSOP, TSSOP
SN75C3232	2 drivers/ 2 receivers	V_{CC}: 3.3 V, 5 V I/O: LVTTL/ RS232 1 Mbit/s	±15 kV HBM ESD (on bus pins)	16-pin SOIC, SSOP, TSSOP
SN75C3238	5 drivers/ 3 receivers	V_{CC}: 3.3 V, 5 V I/O: LVTTL/ RS232 1 Mbit/s	±15 kV HBM ESD (on bus pins)	28-pin SOIC, SSOP, TSSOP
SN75C3243	3 drivers/ 5 receivers	V_{CC}: 3.3 V, 5 V I/O: LVTTL/ RS232 1 Mbit/s	±15 kV HBM ESD (on bus pins)	28-pin SOIC, SSOP, TSSOP
SN75C23243	6 drivers/ 10 receivers	V_{CC}: 3.3 V, 5 V I/O: LVTTL/ RS232 250 kbit/s	±15 kV HBM ESD (on bus pins)	48-pin SSOP, TSSOP

10 TIA/EIA-422

TIA/EIA-422 (RS-422) allows a multidrop interconnection of one driver, transmitting unidirectional to up to 10 receivers. Although it is not capable of bidirectional transfer, it is still applicable and used for talker-audience scenarios.

10.1 Electrical

TIA/EIA-422 (ITU-T V.11) is limited to unidirectional data traffic and is terminated only at the line end opposite to the driver (refer to the multidrop explanation at the beginning of this report). Line length to 1200 m is possible and, over shorter distances, signaling rates of 10 Mbps are common. TIA/EIA-422 allows up to ten receivers (input impedance of 4 kΩ) attached to one driver. The maximum load is limited to 80 Ω while the output needs to supply an amplitude of 2 V minimum. The receivers of TIA/EIA-422 detect the bus state with as little as 200 mV differential and up to 7 V of common-mode signal.

10.2 Protocol

Not applicable/none specified

10.3 Applicability

TIA/EIA-422 is most commonly used in DTE-to-DCE interface in telecommunications but has general applicability to any point-to-point or multidrop bus where a direct connection is desired in the presence of ground noise.

10.4 Features

- Established standard
- Good for multidrop over long distances
- High noise immunity and low radiated emissions

Table 10. Top TIA/EIA-422 Device List

DEVICE	BIT WIDTH	POWER	PACKAGE
AM26LS31	4 drivers	V_{CC}: 5 V I/O: (LV)TTL/RS–422	16-pin PDIP and SOIC
AM26LS32A	4 receivers	V_{CC}: 5 V I/O: (LV)TTL/RS–422	16-pin PDIP and SOIC
SN75ALS192	4 drivers	V_{CC}: 5 V I/O: (LV)TTL/RS–422	16-pin PDIP and SOIC

11 TIA/EIA-485

TIA/EIA-422 was published before TIA/EIA-485. Due to the lack of bidirectional capabilities allowing for multipoint connections, the TIA/EIA-485 standard was created to add this feature. The new standard (TIA/EIA-485 or ISO/IEC 8284) defines the electrical characteristics of the interconnection, including driver, line, and receiver. It allows data rates in the range of 35 Mbps and above, and allows line lengths of up to 1200 m. Of course, both limits cannot be reached at the same time. Recommendations are given regarding wiring and termination. The standard does not specify the connector or any protocol requirements.

11.1 Electrical

TIA/EIA-485 describes a half-duplex, differential transmission method designed for twisted-pair cables and other balanced media. The standard requires drivers to deliver a minimum differential output voltage of 1.5 V with up to 32 *unit loads* of about 12 kΩ each, plus termination resistors at each end of the bus. Connection of more than 32 nodes is possible if fractional unit-load devices are used. The common-mode voltage levels on the bus may vary between –7 V and 12 V and receivers must be sensitive enough to determine the bus state based on a differential signal level of 200 mV.

11.2 Protocol

No particular protocol is specified in the standard. However, many popular protocol standards reference RS-485 as an electrical-layer solution. These include Profibus (EN 50170), Interbus-S, and MODBus.

11.3 Applicability

Due to its differential transmission form, 485 is robust against electrical noise corruption. Due to its wide common-mode voltage range, it is tolerant to ground potential shifts between nodes. For both of these reasons, this standard is perfectly suited for applications requiring low noise emissions and susceptibility. This is especially valuable in long lines. In most applications, the signaling rate is sufficient, for example, to control a process line. TIA/EIA-485 is also used in backplane connections, as its high node-count and data integrity are necessary features for these applications.

11.4 Features

- Very robust interface (common-mode range: −7 V to 12 V)
- Low radiated emissions
- High noise tolerance
- Multiplex mode of operation
- Up to 256 nodes with 1/8th UL transceivers

Table 11. Example TIA/EIA-485 Device List

DEVICE	FUNCTION	POWER	PACKAGE
SN65HVD1x	Single channel transceivers	V_{CC}: 3.3 V I/O: (LV)TTL/RS–485	8–pin SOIC
SN65HVD2x	Single channel, wide common mode transceiver, SN65HVD23, SN65HVD24 with receiver equalization	V_{CC}: 5 V I/O: (LV)TTL/RS–485	8–pin SOIC

12 Controller Area Network (CAN)

The controller area network (CAN) is an International Standardization Organization (ISO) defined serial communications bus originally developed for the automotive industry to replace the complex wiring harness with a two-wire bus. The specification calls for signaling rates up to 1 Mbps, high immunity to electrical interference, and an ability to self-diagnose and repair data errors.

CAN is ideally suited in applications requiring a large number of small messages in a short period of time, with high reliability in rugged operating environments. Since CAN is message based and not address based, it is especially suited when data is needed by more than one location and system-wide data consistency is considered mandatory.

12.1 Electrical

The CAN standard ISO 11898 defines half-duplex, differential transmission on cable lengths up to 40 m, a maximum stub length of 0.3 m, and a maximum of 30 nodes at signaling rates up to 1 Mbps. However, with careful design, longer cables, longer stub lengths, and many more nodes can be added to a bus—always with a trade-off in signaling rate.

A single shielded or unshielded twisted-pair cable with a 120-Ω characteristic impedance (Zo) is specified as the interconnect. This interconnecting cable is terminated at both ends with a resistor equal to the Zo of the line. Nodes are then connected to the bus with unterminated drop cables, or stubs.

Data transmission circuits employing CAN are used in applications requiring a rugged interconnection with a wide common-mode voltage range. Therefore, shielded cable is recommended in these electronically harsh environments, and when coupled with the Standard's −2-V to 7-V common-mode range of tolerable ground noise, helps to ensure data integrity.

12.2 Protocol

The CAN communications protocol, ISO 11898, describes how information is passed between devices on a network, and conforms to the open systems interconnection (OSI) model that is defined in terms of layers. ISO 11898 defines the functions of the lower layers of the OSI model that are performed within a CAN controller. These CAN controller functions are designed for interaction with a higher layer protocol such as CANopen to complete master and slave node communication relationships for bus operation. There is an abundance of plug-n-play CAN programming routines available on the internet from different vendors.

12.3 Applicability

The robust features of CAN make it ideally suited for the many rugged applications to which the CAN protocol is being adapted. Among the applications finding solutions with CAN are automobiles, trucks, trains, busses, airplanes and aerospace, agriculture, construction, mining, and marine vehicles. CAN-based control systems are being used in factory and building automation and embedded control systems for machines, medical devices, domestic appliances and many other applications.

12.4 Features

- Established standard and standardized plug-n-play products
- Fault tolerant—very high short-circuit protection
- Self-diagnosing error repair
- Very robust interface for harsh electrical environments
- Wide common-mode range

Table 12. Example CAN Device List

DEVICE	FEATURES	POWER	PACKAGE
SN65HVD23x CAN Transceiver Family	High temp range and short-circuit protection Low-power standby & sleep modes Wide common-mode Low power	Vcc: 3.3-V I/O: (LV)TTL/CAN	8-pin SOIC
SN65HVD251	High temp range & short-circuit protection Low-power standby Wide common-mode Low cost	Vcc: 5-V I/O: 5-V CMOS/CAN	8-pin SOIC
TMS320LF240x DSP Family	Full CAN controller Low power	Vcc: 3.3-V I/O (LV) TTL/CAN, SPI, SCI	100-pin PZ 144-pin PGE
TMS320F28xx DSP Family	Full CAN controller Low power	Vcc: 3.3-V I/O (LV) TTL/CAN, SPI, SCI	128-pin PBK 176-pin PGF 179-Ball GHH
TMS320F24x DSP Family	Full CAN controller	Vcc: 5-V I/O TTL/CAN, SPI, SCI	64-pin QFP 68-pin PLCC 144-pin LQFP

13 TIA/EIA-644 (LVDS)

Low voltage differential signaling (LVDS) is an approach to achieve higher signaling rates on commonly used media. Since the limitation of the previously known differential standards is mainly related to the maximum achievable slew rate and EMI restrictions, LVDS targets low-voltage swings that are reached much faster, enabling higher speeds, lower EMI , and lower power consumption.

13.1 Electrical

As the name says, LVDS utilizes differential transmission mode and low signal amplitudes. The swing is in the range of only 350 mV, generated on a 100-Ω termination resistor. The driver may also be a current-mode driver forcing an output current between 2.47 mA and 4.54 mA into either one of the two outputs. This benefits in higher speed, lower power consumption and reduced EMI. More information on EMI comparisons can be found at http://www.ti.com. Search on literature number SLLA030. The common-mode range of LVDS is specified as 0 V to 2.4 V, but devices are available that allow for larger offsets (−4 V…5 V). The chart in Figure 14 shows the dependency of the supply current versus the switching frequency for HVD (TIA/EIA-422), LVDS and PECL. As can be seen, the supply current is significantly lower and also the increase over frequency is much lower with the use of LVDS drivers.

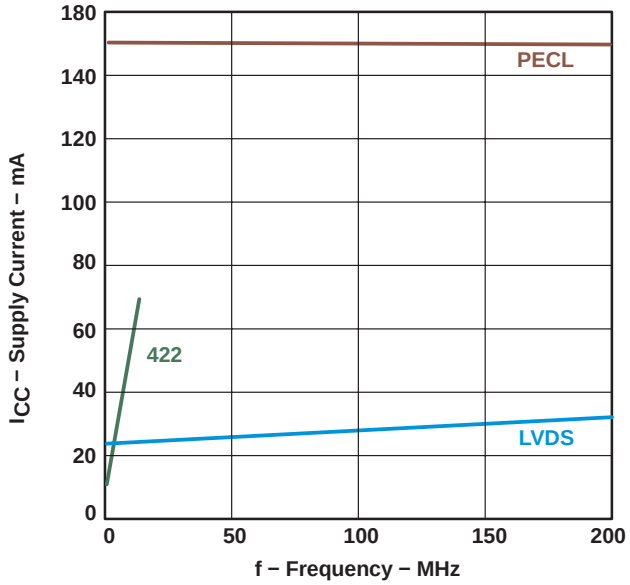


Figure 14. Supply Current Versus Switching Frequency

The initial specification, TIA/EIA-644, addresses only point-to-point interfaces, but it allows the attachment of multiple receivers if attention is paid to several conditions, including stub line length, termination, and signaling rate. Revision A of the standard includes the multidrop option. Most recent devices support transfer rates in the Gbps range (Gigabits per seconds).

13.2 Protocol

TIA/EIA-644 does not specify protocol, but is referenced by higher-level standards.

13.3 Applicability

LVDS targets applications that transfer data point–to–point at very high speeds. It is also capable of driving multiple receivers if care is taken regarding the load configuration. LVDS is particularly suitable for any application that requires low power and/or low EMI. The common-mode input voltage, which is currently limited by the standard to 0 V to 2.4 V, restricts the usage of LVDS with long line lengths (which may cause unpredictable ground shifts), as well as the use in electrically noisy environments. Using Texas Instruments *wide VICR* devices with a significantly increased input voltage range and integrated hysteresis, the applicability in those environments becomes suitable.

In the high-speed range, TI offers repeaters and/or converters for LVDS−PECL / PECL−LVDS translation as well as PECL−CML, LVDS−CML and vice versa. Conversion between LVDS and other levels can be achieved with external circuitry. More detailed information can be found in the application reports SCAA062 and SCAA059 several data sheets, e.g., http://www−s.ti.com/sc/ds/sn65lvds104.pdf . LVDS is found in clock and data distribution, backplane and cable transmission, level conversion and many more applications.

13.4 Features

- Very high speed
- Very low power consumption
- Very low EMI
- Low cost

Table 13. Top LVDS Device List

DEVICE	FUNCTION	POWER	PACKAGE
SN65LVDS33	4-Channel receiver with wide common mode and hysteresis	V_{CC}: 3.3 V I/O: LVTTL/LVDS	16-pin SOIC, 16-pin TSSOP
SN65LVDS387/386	16-Channel driver/receiver	V_{CC}: 3.3 V I/O: LVTTL/LVDS	64-pin TSSOP
SN65LVDS100/101 SN65CML100	Single-channel Gbps LVDS/LVPECL/CML repeater/translator	V_{CC}: 3.3 V I/O: LVDS/LVPECL/CML	8-pin SOIC 8-pin MSOP
SN65LVDS1 SN65LVDT2	Single driver/receiver with integrated termination	V_{CC}: 3.3 V I/O: LVTTL/LVDS	5-pin SOT-23
SN65LVDS/T122/125 SN65LVCP22/23	LVDS/LVPECL 2X2 (4X4) crosspoint switch	V_{CC}: 3.3 V I/O: LVDS/LVPECL	16-pin SOIC 16-pin TSSOP

14 LVDM

LVDM stands for LVDS-multipoint, enabling a half-duplex operation with LVDS voltage levels and speeds. It benefits from the same advantages as LVDS, and additionally allows bidirectional data transfer, and the attachment of several drivers, receivers, and/or transceivers. LVDM is a LVDS-multipoint option available from TI exclusively. Meanwhile, a new standard has been released, following the industry demand for standardized Multipoint-LVDS, including definitions such as bus contention prevention, etc., which are of high importance when mixing devices of multiple suppliers. Please refer to next section, M-LVDS. Devices complying with the new standard provide a higher output drive capability than LVDM. However, for some applications where power consumption and heat sinking are concerns, LVDM might still be an option over M-LVDS. Existing products remain available.

14.1 Electrical

LVDM is LVDS with doubled driver output current. For bidirectional transfers, a termination is needed at each end of the line. The requirement of termination matching the line impedance remains. Therefore, both ends are terminated with 100 Ω. The effective termination resistance results in the parallel configuration of these two resistors, equaling half the impedance or twice the load. To ensure the same input voltage levels, such as with LVDS (i.e. at a 100-Ω load), the output current is doubled to generate the required amplitude on loads of just 50 Ω.

14.2 Protocol

Not applicable/none specified.

14.3 Applicability

LVDM devices are suitable for half-duplex (bi-directional) communications between two nodes at up to 655 Mbps and distances up to 30 m (depending on ground noise).

14.4 Features

- Drives double terminated multipoint
- Very high speed
- Very low power consumption
- Very low EMI
- Low cost

Table 14. Top LVDM Device List

DEVICE	FUNCTION	POWER	PACKAGE
SN65LVDM176	Single-channel transceiver	V_{CC}: 3.3 V I/O: LVTTL/LVDM	8-pin SOIC
SN65LVDM1676 / 1677	16-channel driver/receiver	V_{CC}: 3.3 V I/O: LVTTL/LVDM	64-pin TSSOP
SN65LVDM050	Dual-channel driver/receiver	V_{CC}: 3.3 V I/O: LVTTL/LVDM	16-pin SOIC
SN65LVDM320	Octal latched transceiver	V_{CC}: 3.3 V I/O: LVTTL/LVDM	64-pin TSSOP
SN65LVDM31	Quad driver	V_{CC}: 3.3 V I/O: LVTTL/LVDM	16-pin SOIC

15 M-LVDS

After recognizing the benefits of LVDS, users soon demanded support of the multipoint mode of operation with LVDS-like signals. The technical committees of TIA responded with the development and publication of TIA/EIA-899, multipoint-LVDS or M-LVDS. M-LVDS modifies the electrical specifications of LVDS to accommodate the lower-impedance loads, stubs, failsafe issues, and other problems unique to the multipoint bus structure.

15.1 Electrical

The differential output voltage of a standard M-LVDS driver is 480 mV to 650 mV across a 50-Ω test load and, with a 50-mV receiver threshold, provides a minimum of 430 mV of differential noise margin. This margin allows for loaded bus impedance as low as 30 Ω and reflection coefficients of −0.25. The receiver common-mode input voltage may range from –1 V to 3.4 V.

TIA/EIA-899 specifies two types of receivers. Type-1 receivers have an input threshold near zero volts, while the Type-2 receiver threshold is nominally 100 mV as shown in Figure 15. The option of the Type-2 receiver allows idle-line failsafe to be implemented at the cost of noise margin.

The driver and input characteristics of M-LVDS interfaces are specified such that 32 worst-case loads may be connected to a single bus segment. To allow for the stubs created by these connections, the driver output transition times are limited to be no faster than 1 ns. Additionally, the standard suggests that silicon providers offer different signaling-rate options, so customers can choose according to their specific requirements (limit EMI, allow for longer stub lines, etc).

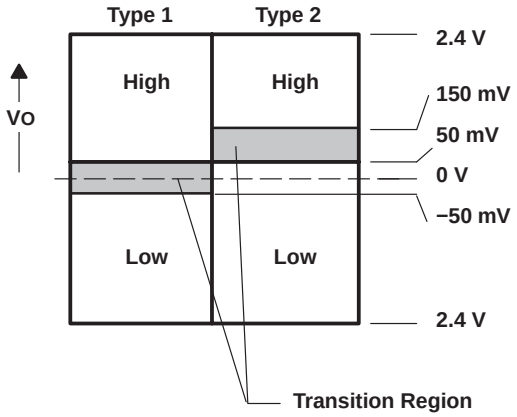


Figure 15. Type 1/Type 2 Switching Levels

15.2 Protocol

Not applicable/none specified.

15.3 Applicability

M-LVDS allows multipoint connection of up to 32 nodes and signaling rates to 500 Mbps. These features make M-LVDS applicable to backplane or cabled data transmission where single-ended or TIA/EIA-485 signaling rates, power consumption, or electromagnetic interference is unacceptable. The common-mode range of M-LVDS likely limits application to cables of 30 meters or less but depends upon the environment.

15.4 Features

- High speed
- Low power consumption
- Low EMI
- Up to 32 bus connections
- Slew-rate-limited driver outputs
- Type-2 receivers available for idle-line failsafe
- Loaded bus impedances as low as 30 Ω
- Capable of live-insertion

Table 15. Top M-LVDS Products

DEVICE	FUNCTION	POWER	PACKAGE
SN65MLVD200/201	100/200 Mbps, half duplex transceiver without failsafe	V_{CC}: 3.3 V I/O: LVTTL/M-LVDS	8-pin SOIC
SN65MLVD202/203	100/200 Mbps, full duplex transceiver without failsafe	V_{CC}: 3.3 V I/O: LVTTL/ M-LVDS	14-pin SOIC
SN65MLVD204/206	100/200 Mbps, half duplex, failsafe transceiver	V_{CC}: 3.3 V I/O: LVTTL/M-LVDS	8-pin SOIC
SN65MLVD205	100 Mbps, full duplex, failsafe transceiver	V_{CC}: 3.3 V I/O: LVTTL/M-LVDS	14-pin SOIC
SN65MLVD080/082	200 Mbps, half duplex, transceiver without/with failsafe	V_{CC}: 3.3 V I/O: LVTTL/M-LVDS	64-pin TSSOP

16 LVDS Serdes and FlatLink™

LVDS serializer-deserializer (serdes) and FlatLink™ technology-based devices physically interconnect two parallel bus systems through a high frequency serial data path using LVDS technology. The following explanations apply to both, LVDS serdes and FlatLink™ type devices; differences are mentioned in the text accordingly.

Principle of a Serdes (serializer/deserializer) Device: The requirement for functionality is a transmitter and a receiver. From a user standpoint, the application is doing nothing more than repeating a number of parallel-clocked data over a longer distance. Therefore, the receiver's output appears to the user the same as the signal seen on the transmitter's input bus. The range for the bus clock rate is limited by the bandwidth of the on-chip PLL (e.g., 30–66 MHz).

The transmitter has a certain number of LVTTL-compatible data input pins (parallel bus) and a clock input. The input pins can be split (i.e., FlatLink™) into different groups. All of the data signals in one group become serialized into a higher frequent data stream. The compression value can be either 7:1 or 10:1, depending on the device. The process can be visualized as a multiplexer switching between all signals of a group running on a frequency equal to the clock multiplied by the number of signals to be transmitted. This serial data stream is sent into a differential pair of lines based on LVDS. The original clock signal is either transferred over an additional pair of lines, or is embedded in the serial data stream and can be recovered on the receiver part (see protocol example).

On the receiving side, the high frequency differential data stream is demultiplexed and clocked out to the parallel LVTTL output bus.

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Table 16. Multiplexing Ratios for LVDS Serdes and FlatLink™ Devices

	INPUT (LVTTL)	OUTPUT (LVDS)
Transmitter	10 data lines + clock line	1 line with embedded clock
	21 data lines + clock line	3 data lines + clock line
	28 data lines + clock line	4 data lines + clock line
Receiver	1 line with embedded clock	10 lines + clock line
	3 data lines + clock line	21 lines + clock line
	4 data lines + clock line	28 lines + clock line

16.1 Electrical

The parallel I/O bus is LVTTL based. The high-speed serial transmission uses LVD-Signaling while meeting or exceeding the ANSI EIA/TIA-644 Standard. The devices require a single 3.3-V power supply.

16.2 Protocol

FlatLink™ devices are optimized for video data transmission (SVGS, XGA and SXGA) between display processor and flat panel display.

There are no specific protocol requirements for using 10-bit LVDS Serdes devices. However, the transmitters are generating a start and a stop bit between each 10 bits sent over serial link. The start/stop bits ensure correct byte boundary on the parallel receiver bus, and sufficient transition density for the clock recovery circuit.

16.3 Applicability

FlatLink™: This technology is designed to transfer large data packets from the CPU to the graphic LCD display in a notebook type of application. The major advantages, compared with realizing this transfer based on standard bus logic, are in reduced number of parallel data lines, reduced power consumption, and lower electromagnetic emission.

LVDS Serdes: The differential transmission mode provides high robustness against in-coupling noise. Therefore, LVDS serdes devices are perfectly suited as point-to-point interconnections between two parallel buses in telecom backplanes, or industrial applications.

Bus speed: The clock rate of those bus systems must be chosen within a defined range. The limiting factor for minimum and maximum clock speed is the fully integrated PLL of the transmitter that needs to lock onto the input clock. The following frequency ranges are supported by TI solutions:

— FlatLink™: 20...65 or 31...68 MHz

— 10-bit LVDS Serdes: 10...40 MHz, 30...66 MHz, and 10...66 MHz

Bus Topology: Serdes can be used as point-to-point or multidrop connections as well as replacing slower bus systems via a daisy chaining architecture.

Initialization after reset/power down: As typical in all PLL based applications, the receiver requires a certain time to lock to the clock signal. Therefore, the result on the receiver output becomes valid after approximately 1 ms.

16.4 Features

- Data throughput up to 660 Mbps over one differential pair
- Industrial temp range (−40°C to 85°C) for LVDS serdes
- Very low power consumption and low emission (portable devices)
- Using a daisy-chain layout offers multidrop architecture ability
- Low power consumption when disabled (below 1 mW)

Table 17. LVDS Serdes Device List

DEVICE	SERDES RATIO	THROUGHPUT	V_{CC} AND I/O	PACKAGE
LVDS serdes				
SN65LV1021/1212 SN65LV1023/1224 SN65LV1023A	10:1	100−400 Mbps 300−660 Mbps 100−660 Mbps	Power supply: 3.3 V Parallel I/O: LVTTL Serial I/O: LVDS	28-pin SSOP
SN65LVDS95/96 SN65LVDS93/94	21:3 28:4	0.420−1.365 Gbps 0.560−1.820 Gbps		48-pin TSSOP
FlatLink™				
SN75LVDS84/84A/86/86A	21:3	0.67−1.428 Gpbs	Power supply: 3.3V Parallel I/O: LVTTL Serial I/O: LVDS	48-pin TSSOP
SN75LVDS82/83	28:4	0.868−1.904 Gpbs		56-pin TSSOP

17 General-Purpose Gigabit Transceivers

General-purpose gigabit transceiver devices have been made to carry a large number of data bits over one differential pair. The input to the transceiver is a parallel 16- or 18-bit wide bus system. These input bus signals are serialized and sent over a differential link to the second transceiver deserializing the serial pattern and clocking it out on a parallel interface again. The input and output bus appears identical to the user.

General-purpose gigabit transceiver products address primary point-to-point high-speed data transfer applications.

17.1 Electrical

The parallel interface of TI's 16:1 general purpose gigabit devices consists of 16 transmit data lines latched on rising edge of a corresponding clock signal and two control signals enabling sending special characters. The receive path is designed in a similar manner: 16 data bits and clock plus two status bits (Figure 16).

The 18:1 general purpose gigabit transceiver accepts 18 bits of data with clock signal on its parallel transmit interface. On the receiving path, 18 bits with recovered clock are present.

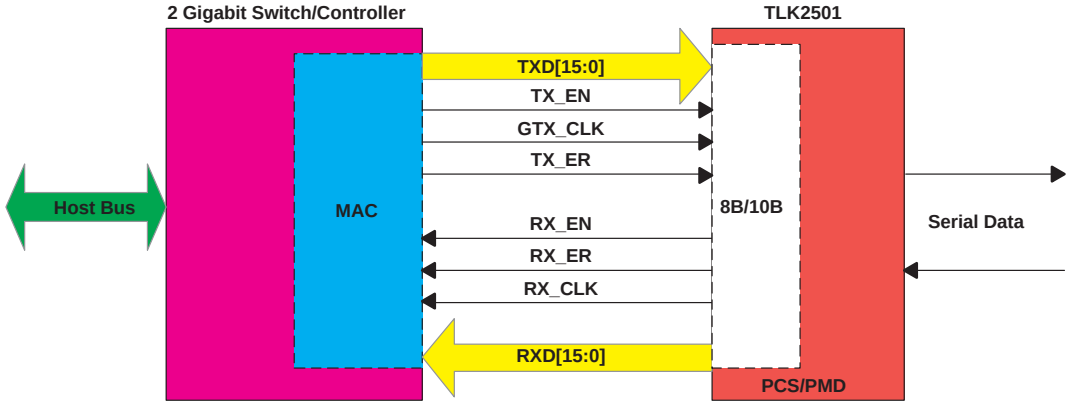


Figure 16. Parallel Interface

Parallel I/O: 3.3-V Tolerant LVTTL Input, 2.5-V LVTTL Output.

Serial link: Historically, there are generally three driver topologies used for data transmission at gigabit speeds: (LV)PECL (Low Voltage Positive Emitter Coupled Logic), CML (Current Mode Logic) and VML (Voltage Mode Logic).

A (LV)PECL driver sources V_{OH} onto a load and provides strong rising edge, but relies on a pull-down resistor for the falling edge.

A CML driver sinks a fixed current into a load – Ohm's law dictates signal swing. CML relies on a pull-up resistor for the rising edge.

VML drives certain V_{OL} and V_{OH} onto a load. The load impedance then determines current flow. VML sources both rising and falling edges of the signal.

TI's CML and VML drivers provide a typical differential swing of 850 mV (LVPECL compatible). Receiver input sensitivity is down to 200 mV.

Functionality: The following steps are performed on the transmitter side of a 16-bit general purpose gigabit transceiver:

1. The incoming bus signal is buffered in reference to the input clock signal
2. 8B10B encoding of the data word (ensuring sufficient transition rate of equal/above three or more transitions on 10-bit data for clock recovery purposes, as well as DC balance of serial data stream, allowing AC coupling)
3. Serialization of the data
4. Clock the serial data into the differential line using the CML/VML driver

The receiver side performs these operations in reverse order, regenerating the original sent word.

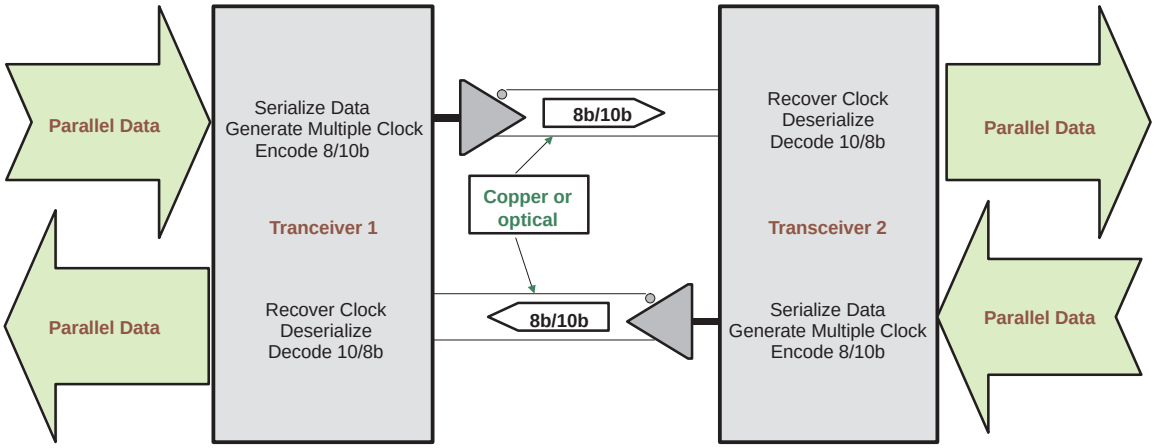


Figure 17. Serdes Interface Using Two Transceivers

Transmission media: The transmission media of the serial path can be PCB, copper cable, or fiber-optics using an optical module between transceivers. The single-ended impedance of the copper must be matched to 50 (75) Ω. The maximum distance to be bridged depends on the transmission speed and the transmission media. Tests have shown proper functionality at 2.5 Gbps over distances up to 10 m of xTP Cat5 cable.

17.2 Protocol

There is no protocol necessary for usage of TI's general-purpose gigabit transceivers.

Using special carrier words and an initialization algorithm, the on-chip state machine of a 16-bit transceiver allows correct data transfer after reset, or data loss. It also ensures the boundary of the parallel output data word out of the incoming serial bit stream. Status outputs on the receiver inform the user about the actual transmission state, as it can be normal data transfer, transmission error, idle, or carrier extension.

There no specific protocol requirements for using 18-bit general-purpose serdes devices. However, the transmitter adds a start and a stop bit between each 18 bits sent over the serial link. This start/stop bits ensure correct byte boundary on the parallel receiver bus and sufficient transition density for the clock recovery circuit.

17.3 Applicability

The differential transmission mode provides high robustness against coupled noise. Therefore, serdes devices are suited for networking, telecommunication, or data-communication designs.

Bus speed: The clock rate of those bus systems can be chosen within a certain range. The limiting factor on minimum and maximum clock speed is the bandwidth of the fully integrated PLL (e.g., 80 -125 MHz).

Bus Topology: Gigabit serdes can be used for point-to-point connections.

Initialization after reset/power down: As typical in all PLL-based applications, the receiver requires a certain time to lock to the incoming serial signal. During this time the receiver output and control pins are held in a high-impedance state for up to one millisecond.

Adjustable voltage swing: The serial output driver offers an adjustable voltage swing being used for optimizing a particular transmission line impedance and length, as well as for controlling the output swing for EMI and attenuation concerns.

17.4 Features

- Data throughput up to 2.5 Gbps over one differential pair
- Very low power consumption, low emission
- External pins to signal data errors/loss of signal on receiving side.
- Integrated clock recovery
- Full duplex data transmission
- Serial link and device test using built-in random bit generator/verification function

Table 18. Serial Gigabit Device List

DEVICE	SERIAL SPEED (DATA THROUGHPUT)	V_{CC} AND I/O	PACKAGE
TLK1501 TLK2501	0.6 - 1.5 Gbps (0.48 - 1.2) 1.6 - 2.5 Gbps (1.28 - 2.0)	V_{CC}: 2.5 V Parallel input 3.3 V tolerant Serial I/O: CML	64-pin VQFP
TLK2701/2711	1.6 - 2.7 Gbps (1.28 - 2.16)	V_{CC}: 2.5 V Parallel input 3.3 V tolerant Serial I/O: CML/VML	64-pin VQFP 80-ball MicroStar™ Junior
TLK3101	2.5 - 3.125 Gbps (2.0 - 2.5)	V_{CC}: 2.5 V Parallel input 3.3 V tolerant Serial I/O: VML	64-pin VQFP
TLK3104SC	3.1 - 3.125 Gbps (2.48 - 2.5)	V_{CC}: 2.5 V Parallel input 4/5 bit LVDS Serial I/O: VML	289-ball PBGA

18 Gigabit Ethernet and Fibre Channel

Gigabit Ethernet standards has been primary developed to provide connectivity among rapidly growing computer networks, e.g., within companies or organizations. Nowadays, it is also widely used for any kind of data communication over glass fiber, copper cables, and backplanes.

Fibre Channel is a channel/network standard containing protocol, connectivity and distance guidelines for high performance storage networks and server interconnections.

18.1 Electrical

IEEE802.3z Gigabit Ethernet standard specifies the physical and the data link layer (in reference to the OSI model) for a serializer/deserializer device running at 1.25 Gbps on serial link. The parallel interface is a ten-bit interface (TBI) with 10 bits of LVTTL data aligned to the rising edge of the clock. The data is already 8B/10B encoded. Serial link is based on LVPECL signaling.

The electrical part of ANSI X3T11 Fibre Channel specification defines using TBI interface on parallel bus and LVPECL on serial link as well.

IEEE802.3ae 10-gigabit Ethernet standard describes, among other things, the 10-Gigabit Media Independent Interface (XGMII) as parallel bus as well as the 10-gigabit attachment unit interface (XAUI) as serial interface. XGMII interface consists of:

- 32 data bits of 1.5-V high-speed transceiver logic (HSTL) Class 1 signals (former drafts of the specification prescribed using 1.8-V HSTL) in each direction
- 4 LVTTL control bits indicating that the reconciliation sublayer is presenting either valid data or control characters
- Corresponding clock signal for sampling and driving both data and control signals, in double data rate (DDR) mode (signals valid on rising and falling edge of clock)

XAUI interface includes four ac-coupled point-to-point differential pairs. The nominal baud rate is 3.125 Gbps with maximum differential voltage of 1.6 V peak-to-peak.

18.2 Protocol

Gigabit Ethernet, 10 Gigabit Ethernet and Fibre Channel standards prescribe using specific protocols for controlled data transmission. Detailed description of these standards is outside the scope of this report.

It is not necessary, however, to provide fully spec-compliant data to the transceiver device (PHY) to ensure its functionality. It is important to know that Gigabit Ethernet and Fibre Channel transceivers expect 8B/10B encoded data on their parallel interfaces (10-gigabit devices can provide on-chip encoding/decoding function), and that they use special pattern − K28.5, for word alignment purposes, on the receiver parallel bus.

18.3 Applicability

Gigabit Ethernet and Fibre Channel protocols are widely used in local area network (LAN) applications for transferring large amounts of data over copper cable or glass fiber. 10-Gigabit Ethernet systems are primary used in metropolitan and wide area networks.

Bus speed: Fibre Channel transceivers work at a fixed speed of 106.25 MHz on the parallel interface; Gigabit Ethernet devices accept 125-MHz parallel data; XGMII works at 156.25 MHz, respectively. However, TI’s Gigabit Ethernet transceivers offer extended parallel clock range. The limiting factor on minimum and maximum clock speed is the bandwidth of the fully integrated PLL.

Bus skew: The output data stream of a Gigabit Ethernet/Fibre Channel transceiver device is device specific and independent of the input bus skew. This might help to overcome bus skew problems.

Bus Topology: All Gigabit Ethernet and Fibre Channel transceivers are used for point-to-point connections.

18.4 Features

- Data throughput up to 2.5 Gbps over one differential pair
- Predefined patterns for controlled data transmission
- External pins to signal data errors/loss of signal on receiving side
- Integrated clock recovery
- Capability to drive data at 3.125 Gbps over lines up to 80 cm of FR4 backplane
- Serial link and device test using built-in random bit generator/verification function

Table 19. Gigabit Ethernet/Fibre Channel Device List

DEVICE	SERDES RATIO	THROUGHPUT	V_{CC} AND I/O	PACKAGE
SN75FC1000B (Fibre Channel transceiver)	10:1 (TBI) Device expects 8B/10B coded data	1.0625 Gbps	V_{DD}: 3.3 V Parallel input 5.0 V tolerant Serial I/O: PECL	64-pin VQFP
TLK1201 TLK2201 (Gigabit Ethernet transceivers)	sel. 10:1 (TBI) or 5:1 DDR Device expects 8B/10B coded data	0.6−1.3 Gbps 1.0−1.6 Gbps	V_{DD}: 2.5 V Parallel input 3.3 V tolerant Serial I/O: CML	64-pin VQFP 80-ball MicroStar™ Junior
TLK31x4SA (XAUI transceivers)	10:1 DDR or 8:1 DDR(XGMII) sel. 8B/10B on-chip	10.0−12.5 Gbps (uncoded: 8.0−10.0)	V_{DD}: 2.5 V Parallel input 1.5 V (1.8 V) HSTL or SSTL_2 class 1 Serial I/O: VML	289-ball PBGA
TLK2206* *in development	5:1 DDR (RTBI) sel. 8B/10B on-chip	6.0−7.8 Gbps (uncoded: 4.8−6.24)	V_{DD}: 1.8 V Parallel input 1.5 V/1.8 V HSTL (data) and 1.8 V/2.5 V LVCMOS (control) Serial I/O: VML	196-ball PBGA
TLK2208 (Octal Gigabit Ethernet transceiver)	10:1 DDR or 5:1 DDR sel. 8B/10B on-chip	8.0−10.4 Gbps (uncoded: 6.4−8.32)	V_{DD}: 1.8 V Parallel input: 1.8 V/2.5 V LVCMOS Serial I/O: VML	289-ball PBGA

19 SONET/SDH Transceivers

Synchronous optical network (SONET) and synchronous digital hierarchy (SDH), are similar standards defining the data speeds, data formats and electrical/optical performance of the link for optical networks. SONET is a US standard while SDH is the European counterpart.

19.1 Electrical

There are several electrical interfaces defined by ANSI and OIF groups for use in SONET/SDH systems. One of them is the Serdes-Framer Interface SFI-4 described in the OIF-SFI4-01.0 specification. This interface consists of the following, and is used by OC-192 devices:

- 16 LVDS data bits in each direction clocked in source-synchronous manner on 622.08 MHz (optional 311.04 MHz DDR) LVPECL clock
- Framer transmit clock signal sourced by serdes device
- Receive loss of synchronization error signal

19.2 Protocol

SONET/SDH standards prescribe using specific protocols for controlled data transmission. Detailed description of these standards is out of scope of this report.

It is not necessary, however, to provide fully spec-compliant data to the transceiver device (PHY) to ensure its functionality. It is important to know, that SONET/SDH transceivers expect scrambled data (scrambling polynomial: $1+x^6+x^7$) on their parallel interfaces.

19.3 Applicability

SONET/SDH technology dominates in wide area networks (WAN). SONET/SDH links are point-to-point optical connections.

Bus speed: SONET/SDH parallel buses work at fixed speeds, such as: 38.88 MHz (OC-3/STM-1), 155.52 MHz (OC-12/STM-4), 311.04 MHz (OC-24/STM-8), 622.08 MHz (OC-48 and 192/STM-16 and 64).

19.4 Features

- Data throughput up to 9.953 Gbps (OC-192/STM-64)
- Worldwide synchronous data transmission enabling adding/dropping of data within one single multiplexing process
- Forward error correction applicable (PHY devices often support FEC speed which differ from the original frequencies)

Table 20. SONET/SDH Device List

DEVICE	SERDES RATIO	THROUGHPUT	V_{CC} AND I/O	PACKAGE
SLK25x1 SLK27x1	4:1	OC-3/12/24/48 OC-3/12/24/48 + FEC	V_{CC}: 2.5 V Parallel input: LVDS (OIF99.102) Serial I/O: CML	100-pin PQFP

20 PCI/CompactPCI

The primary goal of the PCI developers was a low cost, flexible, high performance industry standard local bus architecture. To enable portable systems with PCI bus, low power dissipation also was a requirement. Personal computers have been the first area where the PCI became the standard for local buses. Meanwhile the PCI bus starts to become a major player in the industrial area. For industrial applications the form factor changed to CompactPCI and hot-swap has been included. The PCI special interest group (PCI SIG: http://www.pcisig.com) maintains the specifications of the PCI bus and the PCI industrial computer manufacturers group (PICMG: http://www.picmg.org/) takes care of the CompactPCI specification.

20.1 Electrical

- 32-bit address space
- 32- or 64-bit data path
- 33-MHz and 66-MHz bus clock speed
- Maximum data rate: 1 Gbps for 33-MHz/32-bit bus; 4 Gbps for 66-MHz/64-bit bus
- Two major form factors:
  - Personal Computer: 62-pin connector for 32-bit (Figure 18) and 82-pin connector for 64-bit systems.
  - CompactPCI: Eurocard industry standard, both 3U (100 mm by 160 mm) and 6U (233.35 mm by 160 mm) board sizes (Figure 19)
- CMOS drivers; TTL voltage levels
- 5 V, 3.3 V interoperable
- Reflected wave switching, thus the bus is short. To increase the number of connected devices PCI-to-PCI bridges are necessary. Figure 20 shows a PCI system with 8 PCI buses.
- Direct drive—no external buffers

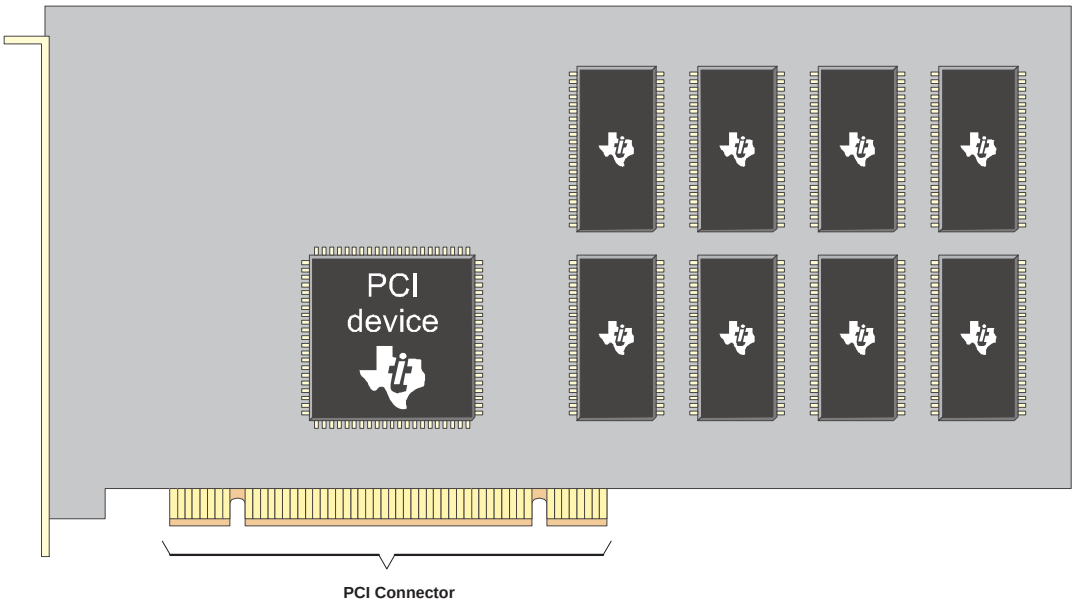


Figure 18. PCI Card for Personal Computer

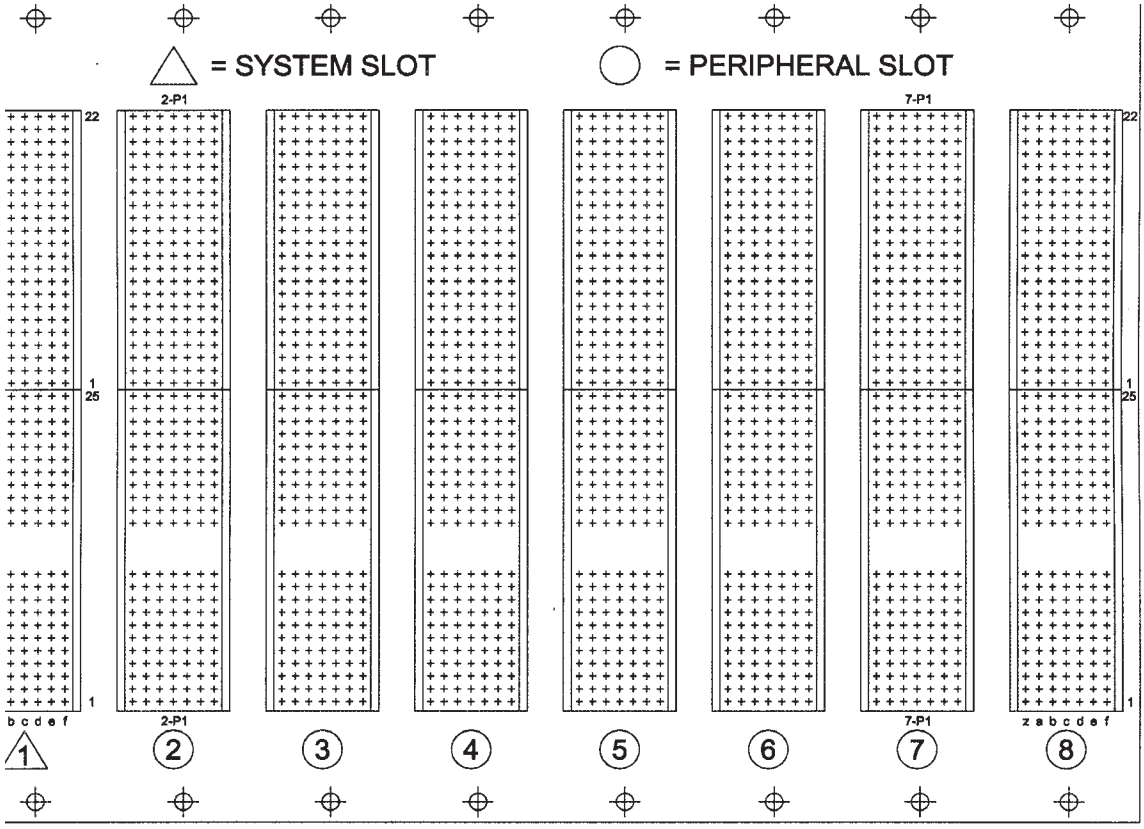


Figure 19. CompactPCI Backplane

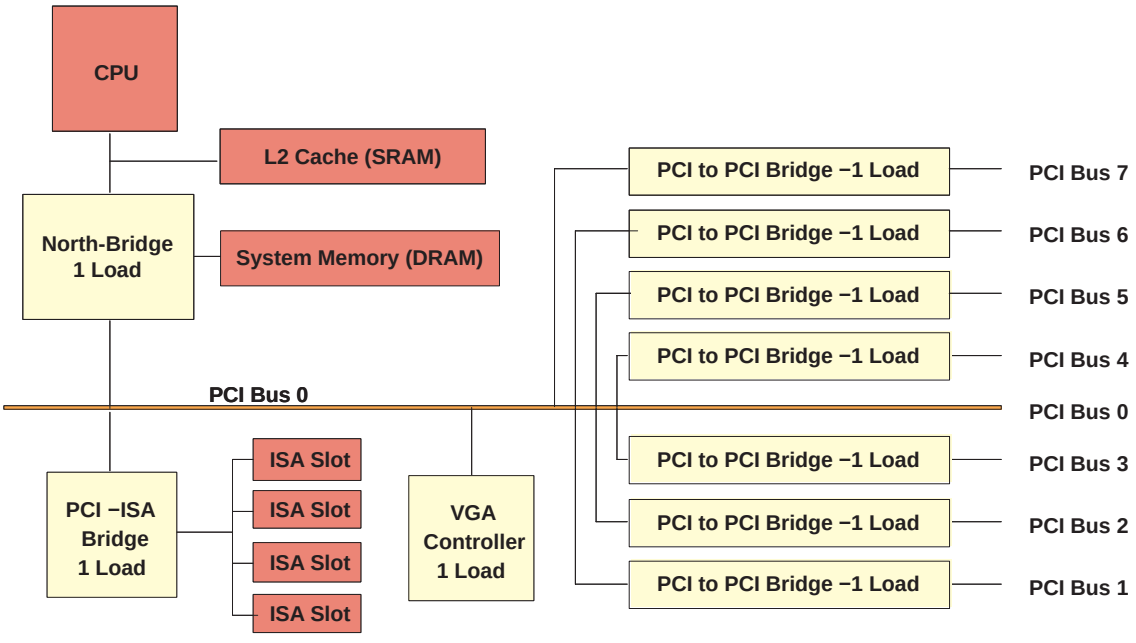


Figure 20. PCI Bus System With 8 PCI Buses

20.2 Protocol

20.2.1 Initialization

PCI devices are not configured after the supply power is switched on. None of the devices have a memory or address range assigned, and no interrupts are available. To operate a PCI bus, all connected devices (master and slaves) have to be configured. Through the configuration space the controller reads the requirements of a device and is able to assign memory-, I/O-space and Interrupts. This enables plug-and-play systems.

In large systems with multiple PCI buses, the configuration software needs an enumerator to number all buses in the system and to program the PCI-to-PCI bridges accordingly.

20.2.2 Operation

During operation each device on the bus may become the master and can transfer data to any other bus member. The bus design requires burst transfers to work efficiently. Still single byte transfers are still possible.

20.3 Applicability

The PCI bus is a computer bus system. The first and biggest success was the personal computer. Nearly every system in the world is equipped with a PCI bus system. High data rates, low cost, multimedia support, and scalability have been key features of the PCI bus that led to the success.

Notebook computers make advantage of the low-power consumption. The reflected wave switching design does not require any termination or additional bus-drivers. The disadvantage is a short bus length that can be increased using PCI-to-PCI bridges. Notebook docking stations often use PCI-to-PCI bridges to generate a new PCI bus in the docking unit.

In the industrial area CompactPCI gains more and more market share. CompactPCI comes in a Eurocard industry standard rack and supports hot-swap. According to the requirements of the industrial environment, high quality connectors with hot-swap support are used for CompactPCI. Besides hot-swap capabilities, the electrical specifications and protocols are identical to PCI. Especially in Telecom and server applications 66 MHz and 64-bit systems are used

20.4 Features

- Processor independent
- Multimaster; peer-to-peer
- Supports memory, I/O, and configuration space
- Data bursting as normal operation mode—both read and write—variable burst length
- Low latency guarantees for real-time devices
- Initialization hooks for auto-configuration
- Arbitration: central,k access oriented, and hidden
- 64-bit extension transparently interoperable with 32 bit

Table 21. Top Device List − PCI Products

DEVICE	SPECIFICATION	DESCRIPTION	PACKAGE	STATUS
PCI1410A	PCI 2.2	PCI-to-CardBus bridge for one cardbus slot	144-pin LQFP 144-pin BGA CSP	Available
PCI1510	PCI 2.2	PCI-to-CardBus bridge for one cardbus slot (successor of PCI1410A)	208-pin LQFP 209-ball PBGA	Available
PCI1420	PCI 2.2	PCI-to-CardBus bridge for two cardbus slots	208-pin LQFP 209-pin BGA CSP	Available
PCI1520	PCI2.2	PCI-to-CardBus bridge for two cardbus slot (successor of PCI1420)	208-terminal LQFP 209-ball PBGA	Available
PCI1620	PCI2.2	PC card, flash media, and smart card controller	209-pin BGA, 208-pin LQFP	Available
PCI4410A		Integrated PC card	209-pin BGA, 208-pin LQFP	Available
PCI4451	PCI2.1/PCI2.2	Integrated PC card	256-pin BGA, 257-pin BGA	Available
PCI4510A	PCI2.2	PC card and integrated 1394a-2000 OHCI two-port-PHY/link-layer controller	209-pin BGA, 208-pin LQFP	Available
PCI4520	PCI2.2	Two slot PC card and integrated 1394a-2000 OHCI two-port-PHY/link-layer controller	257-pin BGA, 257-ball PBGA	Available
PCI6420	PCI2.3	Integrated 2-slot PC card and dedicated flash media controller	288-pin BGA, 288-pin BGA Microstar	Available
PCI6620	PCI2.3	Integrated 2-slot PC card with Smartcard & dedicated flash media controller	288-pin BGA, 288-pin BGA Microstar	Available
PCI7410	PCI2.3	PC card, flash media, integrated 1394a-2000 OHCI 2-port PHY/link-layer controller	209-pin BGA, 208-pin LQFP	Available
PCI7420	PCI2.3	Integrated 2-slot PC card, dedicated flash media socket & 1394a-2000 OHCI 2-port PHY/link-layer controller	288-pin BGA, 288-pin BGA Microstar	Available
PCI7510	PCI2.3	Integrated PC card, smart card, and 1394 controller	209-pin BGA, 208-pin LQFP	Available
PCI7610	PCI2.3	Integrated PC card, smart card, flash media, 1394a-2000 OHCI 2-port-PHY/link-layer controller	209-pin BGA, 208-pin LQFP	Available
PCI7620	PCI2.3	Integrated 2-slot PC card with smart card, flash media, 1394a-2000 OHCI 2-port-PHY/link-layer controller	288-pin BGA, 288-pin BGA Microstar	Available
PCI2040	PCI 2.2	PCI-to-DSP bridge	144-pin LQFP 144-pin BGA CSP	Available
PCI2250	PCI 2.2	PCI-to-PCI bridge, 32-bit, 33 MHz, 4 secondary master	160-pin LQFP 176-pin LQFP	Available
PCI2050B	PCI2.2	PCI-to-PCI bridge, two 32-bit, 66-Mhz PCI buses, 9 secondary masters	257-pin BGA, 208-pin LQFP, 208-pin QFP	

21 IEEE 1284 Compatible Devices

The IEEE 1284 standard provides an open path for communication between computers and intelligent printers and peripherals. The release of the standard signaling method for a bidirectional parallel peripheral interface for personal computers defines a common standard for bidirectional parallel communications between personal computers and peripherals. Preexisting methods used a wide variety of hardware and software products, each with unique, and in most cases, incompatible signaling schemes. As an example, the Centronics printer port is mentioned. There has never been an official standard for this printer port. Therefore, problems in circuit designs occurred due to unknown hardware design elements, such as termination resistors or driver output impedance. For safe data transmission, only a short cable between host and peripheral (1 to 2 m) was acceptable. The release of the IEEE1284 standard answers the demand for an industry-wide, high-speed, high-integrity parallel port standard for a bidirectional peripheral interface. Texas Instruments offers three bus drivers. They support reliable data transfer via cables lengths up to 10 meter (30 feet) at a speed of 16 Mbps.

21.1 Electrical

The IEEE1284 specification defines the physical set up of the 1284 interface including wiring diagram, minimum drive capabilities and termination considerations.

21.2 Protocol

The protocol is defined in the IEEE1284 standard.

21.3 Applicability

The ’1284-compatible devices are widely used from computer and peripheral manufacturers, because the ’1284 standard can communicate more than 50 times faster than conventional parallel port interfaces.

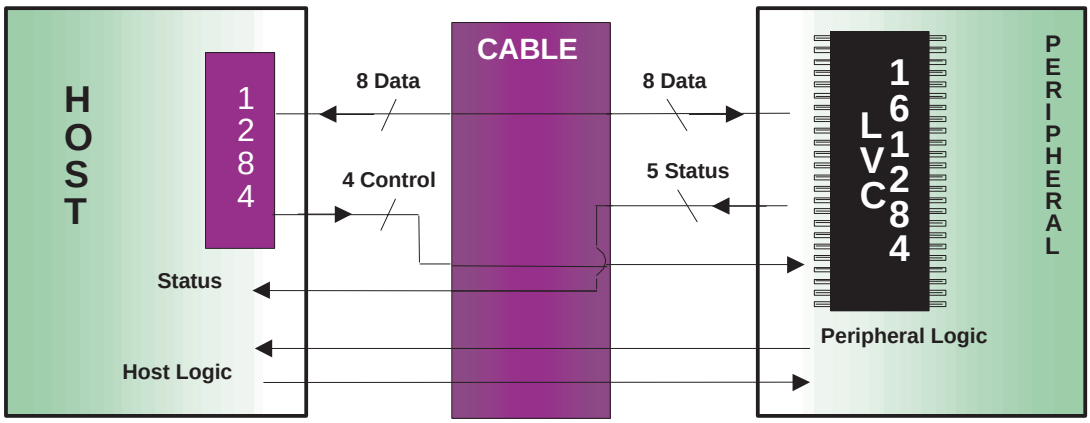


Figure 21. Typical Application Showing a 1284 Interface

21.4 Features

- Designed for the IEEE Std 1284-I (Level 1 Type) and IEEE Std 1284-II (Level 2 Type) electrical specifications
- Adds bidirectional capabilities to the existing Centronics parallel interface
- Supports 5 modes of data transfer (Centronics; Nibble; Byte; EPP; ECP)
- Advanced operating mode can reach speeds of 16 to 32 Mbps
- New electrical interface, cabling and connector for improved performance and reliability while retaining backward compatibility
- 50 to 100 times faster than the original parallel port (Centronics)

Table 22. Top Device List − IEEE 1284-Compatible Devices

DEVICE	SPECIFICATION	DESCRIPTION	PACKAGE	STATUS
SN74ACT1284	TTL	7-bit bus interface with 3-state outputs	20-pin SOP 20-pin SSOP 20-pin TSSOP	Available
SN74LVC161284	LVTTL	19-bit bus interface	48-pin SSOP 48-pin TSSOP	Available
SN74LV161284	LVTTL	19-bit bus interface	48-pin SSOP 49-pin TSSOP	Available

22 General-Purpose Interface Logic at 5 V and 3.3 V

For a long time TTL buses have been the standard solution for backplane systems. Different logic families are available to fulfill the requirement for backplane buses. The choice for the appropriate logic strongly depends on physical characteristics of the bus. The main factor is the number of receiving and transmitting modules connected into that bus. The more cards on the backplane, the lower the impedance of the bus due to additional capacitive loading. This arises from the input/output capacitance of the transceivers, the capacitance layer of printed-circuit stub lines and the connectors, resulting in the need for a higher drive capability of the logic device.

Mature 5-V TTL and 5-V CMOS as well as 3.3-V CMOS technologies provide a drive capability of 24 mA and can only handle line impedance down to about 50 Ω. With the introduction of BiCMOS technologies the drive has been enlarged to −32/64mA and with so called incident wave switching drivers (SN74ABT25xxx) it is even possible to drive bus lines with an impedance as low as 25 Ω. The enhanced transceiver logic (ETL) features improved noise margins, while maintaining compatible TTL switching levels and therefore enabling higher speed on the backplane.

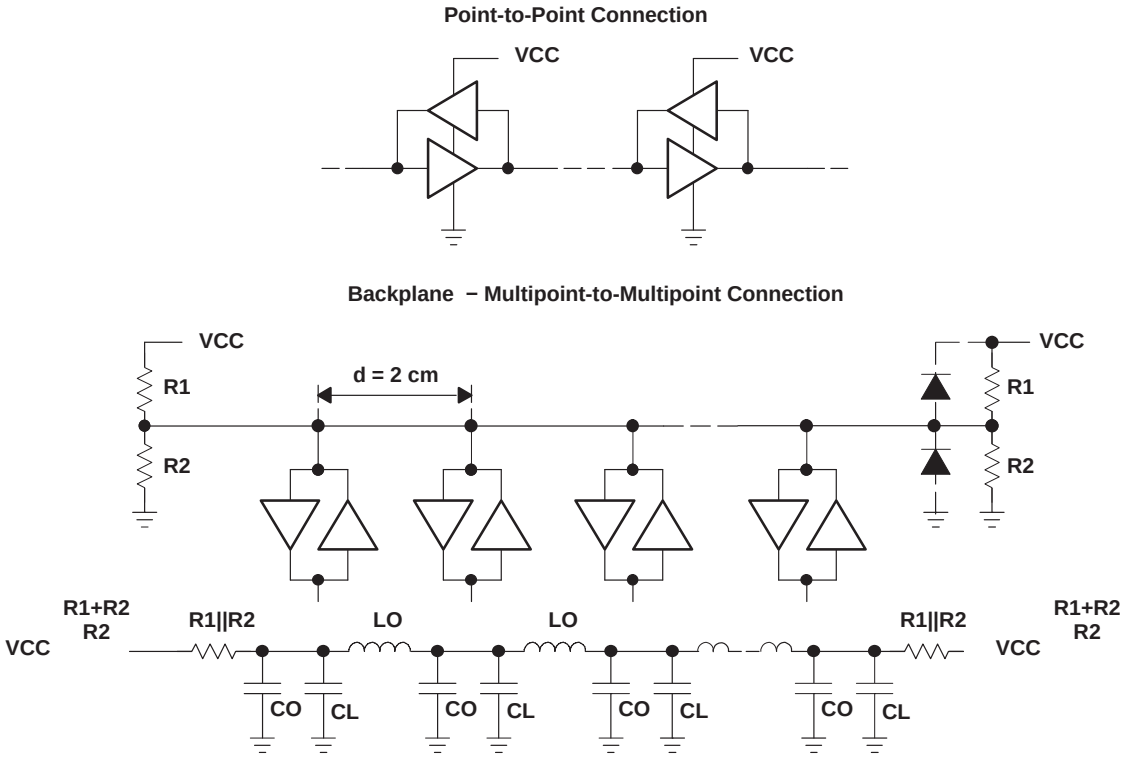


Figure 22. Equivalent Circuit of a Single Backplane Connection

Standard logic devices can be used for either point-to-point connections or to realize backplane buses, which consist of many drivers and receivers along the bus, as shown in Figure 22. Both solutions using standard logic devices are usually set up as parallel buses; up to 36 bits can be switched by one logic device. The operational frequency can be chosen within a range from a few MHz up to the clock frequency of about 50 MHz, such that the data-throughput per device is in the range of 1 to 2 Gbps.

22.1 Electrical

The electrical specification of LVTTL levels meets the TTL specification. The combination of 5-V TTL with LVTTL is possible without any additional effort. 5-V CMOS levels are not compatible with LVTTL levels: 5-V tolerance is mandatory for unidirectional; and the use of 5-V level shifters is required for bidirectional data transfer when combining a 3.3-V system with a 5-V supplied system part. Table 23 shows the key parameters for 5-V and 3.3-V advanced system logic families. Another important feature is the live insertion capability of a logic family, which enables the user to insert and remove modules during operation. The important parameters are IOFF, Powerup/down 3-state, and precharge functionality as shown in Table 23. To get more information about this topic, refer to the application report *Live Insertion* (literature number SCZAE07).

Table 23. Selected Characteristics for General-Purpose Logic Families

FAMILY	RECOMMENDED SUPPLY VOLTAGE	DRIVE (mA)	LEVELS	INTERFACING TO (LV) TTL	LIVE INSERTION, REMOVAL HOT INSERTION
AHC	5 V	±8	5 V CMOS	Use level shifter	
AC	5 V	±24	5 V CMOS	Use level shifter	
ABT	5 V	−32/+64	TTL	Yes	I_{OFF}, PU/D–3-state
ABT25	5 V	−80 (32)/+188 (64)			
ABTE	5 V	−60 (12)/ +90 (12)	ETL	Yes	I_{OFF}, PU/D–3-state and precharge
LVC	3.3 V	±24	LVTTL	Yes	I_{OFF}, (LVCZ: PU/D–3-state)
ALVC	3.3 V	±24	LVTTL	Yes	
LVT	3.3 V	-32/ +64	LVTTL	Yes	I_{OFF}, PU/D–3-state
ALVT	3.3 V	-32/ +64	LVTTL	Yes	I_{OFF}, PU/D–3-state
AVC	2.5 V	±12 +DOC™	2.5 CMOS	Yes	I_{OFF}, PU/D–3-state
AUC	1.8 V	±8	1.8 CMOS	Yes	I_{OFF}, PU/D–3-state

A maximum bus length is not specified for backplanes. However, in practice, the bus length of parallel backplanes does not exceed about 50 cm.

22.2 Protocol

Not strictly specified for standard logic families. VME is applicable. ABTE supports VME64.

22.3 Applicability

The backplanes are not limited to any special domain. They are used in telecom, computer, and industry application, wherever several system parts are connected using a backplane or a memory bus.

22.4 Features

- 8-, 16-, and 32-bit devices enable parallel operation on the backplane/memory bus
- Boundary scan devices (JTAG - IEEE 1149.1) available in LVT and ABT enable easy testability during design and production
- Bus hold feature eliminates external pullup resistor
- Series damping resistors enable improved signal integrity in point-to-point buses

- ABT, LVT, ALVT and LVCZ incorporate power up 3-state outputs, enabling support of hot insertion/removal
- ABTE supports precharge feature, enabling support of hot insertion/removal
- LVC, ALVC are specified down to 1.8 V, further reducing power consumption

Table 24. Top Feature List of Advanced System Logic by Logic Family

	AHC	AC	ABT	ABTE	(A)LVC	LVT	ALVT	AVC	AUC$^{\Phi}$
Gates	n	n	n	N/A	n	N/A	N/A	N/A	n
Flip-flops	n	n	n	N/A	n	n	n	N/A	n
Drivers	n	n	n	n	n	n	n	n	n
Transceivers	n	n	n	n	n	n	n	n	n
UBT™†	N/A	N/A	n	N/A	n	n	n	n	n
Bus hold‡	N/A	N/A	n	n	n	n	n	n	n
26 Ω Series resistors§	n	n	n	n	n	n	n	DOC™	n
SCOPE™¶	N/A	N/A	n	N/A	N/A	n	N/A	N/A	N/A

† The universal bus transceiver (UBTTM) combines D-type latches and D-type flip-flops for operation in transparent, latched or clocked mode.
‡ Bus hold on data inputs eliminates the need for external pullup resistors.
§ 26-Ω series resistors are included in the output stages, in order to match bus impedance avoiding external resistors
¶ SCOPE™ products are compatible with the IEEE Standard 1149.1–1990 (JTAG) test access port and boundary scan architecture

Figure 23 shows a typical backplane application with several plug-in cards.

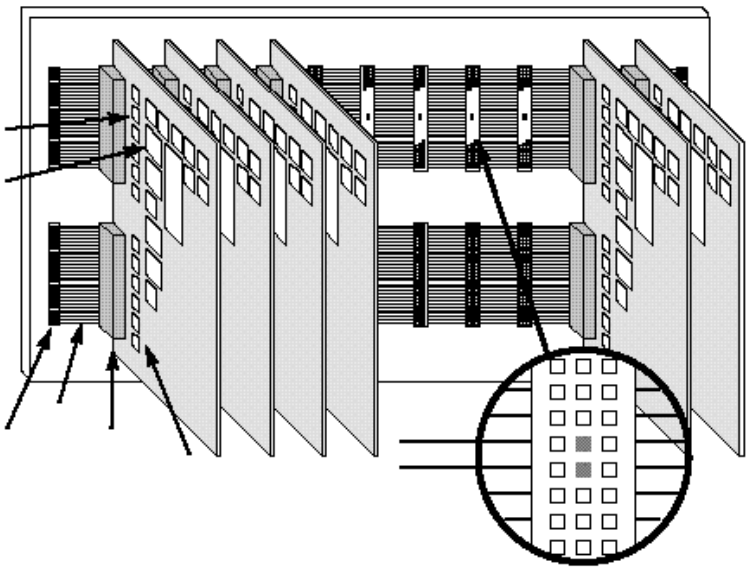


Figure 23. Typical Backplane Application Using Several Plug-In Cards

23 Backplane Transceiver Logic (SN74FBxxx)

In the past, the standard solutions for driving bus lines on backplane systems were TTL or CMOS logic circuits. However, some issues result from the high voltage swing of 3.3 V up to 5 V. Correct termination for all load conditions is not possible and large drive capabilities are necessary to enable incident wave switching.

A bus system with reduced voltage swing solves a lot of problems. The BTL bus realizes a bus in open collector mode, as shown Figure 24. In this case, the falling edge is actively generated from the driver. Only a low impedance driver can switch the bus with the incident wave.

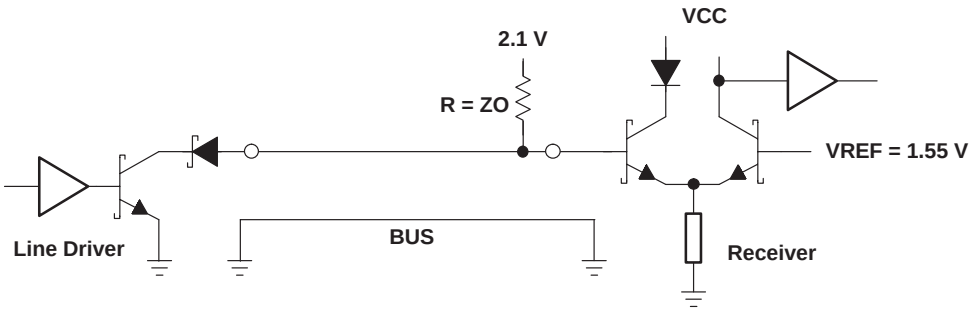


Figure 24. Principle Setup of an Open Collector Bus System Using BTL Devices

23.1 Electrical

The physical layer of the Futurebus is called backplane transceiver logic (BTL) and works with a voltage swing of 1.1 V only, using an open collector bus system. The saturation voltage of the pulldown transistor and the forward voltage of the serially connected diode generates the output low level voltage of 1 V. The high level of 2.1 V comes from the termination resistor connected to the termination voltage of 2.1 V. The value of the termination resistor is equal to the impedance of the bus line and therefore the bus line is terminated correctly. For safe detection of the logic levels, the inputs are designed with differential amplifiers and a threshold at 1.55 V, exactly in the middle of the voltage swing.

To reduce I_{CC} current spikes, the fall time is defined to be 2 ns or slower. The rise time is not generated by active electronics, but by the pullup resistor.

23.2 Protocol

The FutureBus + logical layer specification, according to IEEE896.2, describes the node management, live insertion, and profiles. However, the physical layer may also be used stand-alone without the logical layer.

23.3 Applicability

The target area for BTL devices is the telecom sector, where live insertion capability is mandatory.

23.4 Features

- Reduced voltage swing: V_L = 1 V; V_H = 2.1 V generates low switching noise 10 Ω (20 Ω || 20 Ω) line impedance
- Correct line termination by a pullup resistor at the line end avoids line reflections
- Decoupling diode reduces output capacitance to < 5 pF, increases line impedance
- Maximum output edge rate 2 ns; trapezoidal waveform reduces system noise
- Supports live insertion/withdrawal

Table 25. Top Device List − Backplane Transceiver Logic

DEVICE	SPECIFICATION	DESCRIPTION	PACKAGE	STATUS
SN74FB2033A	TTL/BTL	8-Bit TTL/BTL registered transceivers	52-pin PQFP	Available
SN74FB1651	TTL/BTL	17-Bit TTL/BTL universal storage transceivers with buffered clock times	100-pin SQFP	Available
SN74FB2031	TTL/BTL	9-Bit TTL/BTL address/data transceivers	52-pin PQFP	Available
SN74FB1653	LVTTL/BTL	17-Bit LVTTL/BTL universal storage transceivers with buffered clock lines	100-pin SQFP	Available
SN74FB2041A	TTL/BTL	7-Bit TTL/BTL transceivers	52-pin PQFP	Available
SN74FB2040	TTL/BTL	8-Bit TTL/BTL transceivers	52-pin PQFP	Available

24 Gunning Transceiver Logic (SN74GTLxxx) − SN74GTL1655

The basic concept of a GTL bus is similar to a BTL system and is shown in Figure 25.

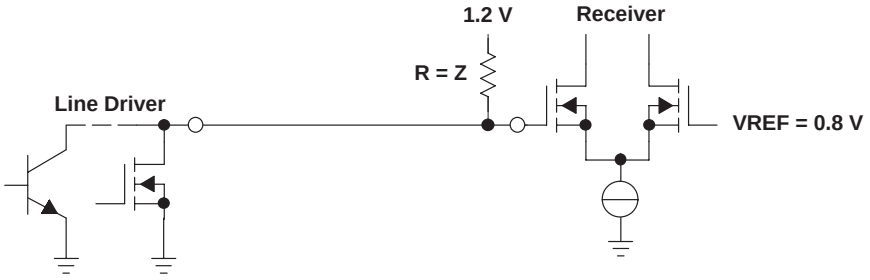


Figure 25. Principle Setup of an Open Collector Bus System Using GTL Devices

Because there is no diode in the open collector/drain outputs (compared to the BTL- solution) the low level is 0.4 V. With a chosen high level of 1.2 V, the voltage swing is reduced to 0.8 V only. Again, the threshold is in the middle of the voltage swing at 0.8 V.

With a drive capability of GTL outputs up to about 40 mA, the GTL devices are able to drive a termination resistor of 0.8 V/40 mA = 20 Ω. If the bus line is terminated correctly, the lowest impedance that can be driven by a GTL driver in the middle of a bus is 40 Ω (effectively the driver sees: 40 Ω || 40 Ω = 20 Ω). As a result of the 0.8 V swing and the 40 mA I_{OL}, the maximum power dissipation of one output is 16 mW. Therefore, it is possible to integrate these low power drivers into ASICs.

24.1 Specialties of the GTL Device SN74GTL1655

With the SN74GTL1655 the benefits of the BTL family and GTL family are combined within one device. The drive capability of the SN74GTL1655 outputs now provides up to 100 mA, enabling the outputs to drive a termination resistor of 11 Ω.

With the GTL1655, even heavily loaded backplane buses can be served. For those buses, the line impedance can decrease down to 22 Ω.

All the features for live insertion and withdrawal have also been included in the GTL1655. The SN74GTL1655 further includes a selectable edge rate control circuit (ERC) for variable rise and fall rates so that the designers can fine tune their circuits for maximum data throughput as system loading dynamically changes. The edge rate control minimizes bus-settling time.

24.2 Electrical

The gunning transceiver logic (GTL) devices support two different logic level specifications: GTL (according EIA/JEDEC Standard EIA/JESD8-3) and the GTL + levels. The bus system, similar to the BTL bus, is realized as an open collector bus. Because no diode is included in the open collector/drain output stage of the GTL devices, the output low level can be reduced to 0.4 V (GTL+: 0.55). With a chosen high level of 1.2 V for GTL (GTL+: 1.5 V), the voltage swing is reduced to only 0.8 V (0.95 V). The threshold is in the middle of the voltage swing at 0.8 V (GTL+: 1 V).

GTL+ is becoming more and more a standard in the industry due to the enlarged noise margin of GTL+ levels. For example GTL+ levels are being used on the Intel Pentium Pro (P6) processor to address this noise margin concern. Using GTL+ levels instead of GTL, the margin is increased about 16 %.

24.3 Protocol

Not specified.

24.4 Applicability

GTL was originally designed for a small bus on a board, for example, between a processor and its memory modules. Because the target application for GTL is not a backplane bus, but a bus on a board, no requirements for live insertion/withdrawal have been included in the specification.

With reduced output levels and state-of-the-art designs, the consequences are reduction of power consumption, higher speeds, and improved signal integrity compared to the BTL-bus, such that GTL+ backplane optimized-drivers are a premium solution for heavily loaded bus systems. Live insertion capabilities and an increased drive for low impedance backplanes are met with the GTL1655 device.

24.5 Features

- Differential amplifier specifies stable threshold voltage of the receiver
- Low voltage swing generates low switching noise
  - GTL: V_L = 0.4 V; V_H = 1.2 V
  - GTL+: V_L = 0.55 V; V_H = 1.5 V
- High drive capable option available, enabling incident wave switching as low as 10 Ω (20 Ω || 20 Ω) line impedance
  - GTL/GTL+: Low drive capability, I_{olmax} = 40/50 mA
  - GTL1655: High drive capability, I_{olmax} = 100 mA
- Correct line termination using a pullup resistor at the line end avoids line reflections
- Edge rate control output circuit of GTL1655 enables variable output slew rate depending on load condition for maximum data throughput.

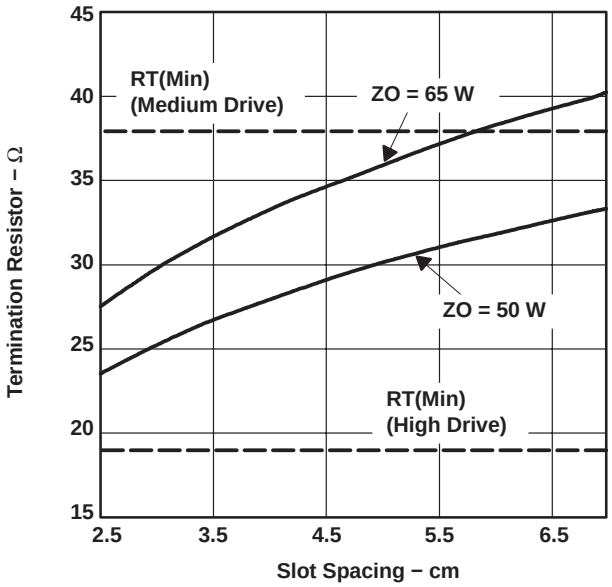
Table 26. Top Device List GTL

DEVICE	SPECIFICATION	DESCRIPTION	PACKAGE	STATUS
SN74GTL16612	LVTTL/GTL	18-Bit LVTTL/GTL+ universal bus transceivers, like 16601 function	56-pin SSOP 56-pin TSSOP	Available
SN74GTL1655	LVTTL/GTL	17-Bit LVTTL/GTL+ universal bus transceivers with live insertion, like 16501 function	64-pin TSSOP	Available
SN74GTL16616	LVTTL/GTL	16-Bit LVTTL/GTL+ universal bus transceivers with buffered clock outputs, like 16601 function	56-pin TSSOP 56-pin SSOP	Available
SN74GTL16622A	LVTTL/GTL	18-Bit LVTTL/GTL+ bus transceivers, like 16601 function without LE and two CE	64-pin TSSOP	Available
SN74GTL16923	LVTTL/GTL	18-Bit LVTTL/GTL+ bus transceivers, like 16601 function without LE and two OE	64-pin TSSOP	Available

25 Gunning Transceiver Logic Plus (SN74GTLPxxx)

GTLP devices are high-speed transceivers (LVTTL/card and GTLP/backplane) that operate like the GTL family except for two major differences: they have been optimized for the distributed loads found in multislot backplanes and they support live insertion with internal precharge circuitry. The GTLP reduced output swing (< 1 V) and reduced input threshold levels allow higher backplane clock frequencies, increasing the bandwidth for manufacturers developing next generation telecommunication and data communication solutions. GTLP devices are backward compatible with commonly used parallel backplane technologies such as ABT, FCT, LVT, ALVT, and FB+ and provide an alternative to more complex serial technologies.

GTLP offers two different drives, 50 and 100 mA recommend I_{OL} at 0.55 V, to allow the designer flexibility in matching the device to backplane length, slot spacing and termination resistor. The medium drive device can drive lines in point-to-point configurations down to 19 Ω. The lowest termination resistor that can be driven by the driver in the middle of a bus is 38 Ω (effectively the driver's load is 38 Ω || 38 Ω = 19 Ω). The high drive devices can drive loads of 9.5 Ω (0.95 V/ 100 mA). So the minimum termination resistor for bus configuration is 19 Ω. It is important to pick a termination resistor that matches the backplane impedance for best signal integrity, but is within the capacity of the driver. Impedance is a function of natural trace impedance (Z_O), stub length, connector impedance, device impedance, and card spacing. Closer spacing reduces the effective impedance, which requires a smaller termination resistor as shown in Figure 26.



NOTE: Assumption: 12 pF/card

Figure 26. R_T vs Slot Spacing With GTLP Medium and High Drive Devices

To enhance the data throughput of a GTLP backplane a source synchronous clock layout is advised. Due to the fact that the clock signal is sent from the same source, the flight time over the bus can be eliminated in the timing budget. This roughly doubles the data throughput of the backplane. TI offers special devices the GTLPH1627 and GTLPH16927 which have one bit integrated for the source synchronous clock. It also features a flexible setup time adjustment (FSTA), which offers the designer an easy way of implementation of a source synchronous bus.

25.1 Electrical

Optimized for the GTLP signal level specifications, also operates at GTL (according JEDEC Standard JESD8-3) or GTL+ signal levels. The bus system, identical to the GTL bus, is realized as an open drain bus. The GTLP voltage swing is from 1.5 V to 0.55 V with ± 50 mV around the V_{REF} threshold of 1 V.

25.2 Protocol

Not specified.

25.3 Applicability

GTLP is used where the major concerns are higher data throughput, live insertion capability or lower power consumption in parallel backplane architectures. GTLP offers up to four times the performance of TTL devices in backplane upgrade applications.

25.4 Features

- 3.3-V operation with 5-V-tolerant LVTTL inputs/outputs which allow the devices to act as 5-V TTL to GTLP as well as 3.3-V LVTTL to GTLP translators
- Significantly improved output edge control (OEC) circuitry on the rising and falling edge of the GTLP outputs reduces line reflections, electromagnetic interference (EMI) and improves overall signal integrity allowing clock frequencies in excess of 80 MHz, with Source Synchronous Clock Layout even in excess of 120 MHz.
- Fully supports live insertion with I_{off}, PU3S and BIAS V_{CC} circuitry
- Edge rate control (ERC) circuitry on high drive devices allows fast or slow edge rates.
- Output edge control (OEC) circuitry on the rising and falling edge of the GTLP outputs
- CMOS construction for 1/3 the static power consumption of BiCMOS logic devices
- A-port (LVTTL side) balanced drive of ±24 mA with optional bus-hold circuitry

Table 27. Top Device List GTLP

DEVICE	SPECIFICATION	DESCRIPTION	PACKAGE	STATUS
SN74GTLPH306	LVTTL/GTLP	8-bit LVTTL/GTLP medium drive bus transceivers	24-pin SOIC 24-pin TSSOP 24-pin TVSOP	Available
SN74GTLP817	LVTTL/GTLP	GTLP/LVTTL medium drive with ERC 1:6 fan out driver	24-pin SOIC 24-pin TSSOP 24-pin TVSOP	Available
SN74GTLP2033	LVTTL/GTLP	8-bit registered transceiver with split LVTTL port and feedback path and ERC	48-pin TSSOP 48-pin TVSOP 56-ball VFBGA	Available
SN74GTLP2034	LVTTL/GTLP	8-bit registered transceiver with split LVTTL port and feedback path and ERC	48-pin TSSOP 48-pin TVSOP 56-ball VFBGA	Available
SN74GTLP21395	LVTTL/GTLP	Two 1-bit transceiver with split LVTTL port, feedback path and selectable polarity	20-pin SOIC 20-pin TSSOP 20-pin TVSOP 20-ball VFBGA	Available
SN74GTLP22033	LVTTL/GTLP	8-bit registered transceiver with split LVTTL port and feedback path and ERC	48-pin TSSOP 48-pin TVSOP 56-ball VFBGA	Available

Table 27. Top Device List GTLP (Continued)

DEVICE	SPECIFICATION	DESCRIPTION	PACKAGE	STATUS
SN74GTLP22034	LVTTL/GTLP	8-bit registered transceiver with split LVTTL port and feedback path and ERC	48-pin TSSOP 48-pin TVSOP 56-ball VFBGA	Available
SN74GTLPH16912	LVTTL/GTLP	18-bit LVTTL/GTLP medium drive universal bus transceivers	56-pin TSSOP 56-pin TVSOP	Product Preview Available
SN74GTLPH16916	LVTTL/GTLP	17-bit LVTTL/GTLP medium drive universal bus transceivers with buffered clock outputs	56-pin TSSOP 56-pin TVSOP	Available
SN74GTLPH16927	LVTTL/GTLP	18-bit LVTTL/GTLP medium drive transceiver with source synchronous clock outputs, FSTA	56-pin TSSOP 56-pin TVSOP	Product Preview
SN74GTLPH16945	LVTTL/GTLP	16-bit LVTTL/GTLP medium drive bus transceivers	48-pin TSSOP 48-pin TVSOP	Available
SN74GTLPH32912	LVTTL/GTLP	36-bit LVTTL/GTLP medium drive universal bus transceivers	114-ball LFBGA	Available
SN74GTLPH32916	LVTTL/GTLP	34-bit LVTTL/GTLP medium drive universal bus transceivers with buffered clock outputs	114-ball LFBGA	Available
SN74GTLPH32945	LVTTL/GTLP	32-bit LVTTL/GTLP medium drive universal bus transceivers	96-ball LFBGA	Available
SN74GTLP1394	LVTTL/GTLP	2-bit LVTTL/GTLP high drive bus transceivers with ERC	16-pin SOIC 16-pin TSSOP 16-pin TVSOP	Available
SN74GTLP1395	LVTTL/GTLP	Two 1-bit LVTTL high drive bus transceivers with ERC	20-pin SOIC 20-pin TSSOP 20-pin TVSOP 20-ball VFBGA	Available
SN74GTLPH1612	LVTTL/GTLP	18-bit LVTTL/GTLP high drive universal bus transceivers with ERC	64-pin TSSOP	Available
SN74GTLPH1616	LVTTL/GTLP	17-bit LVTTL/GTLP high drive universal bus transceivers with buffered clock outputs	64-pin TSSOP	Available
SN74GTLPH1627	LVTTL/GTLP	18-bit LVTTL/GTLP high drive transceiver with source synchronous clock outputs, FSTA	56–pin TSSOP 56–pin TVSOP	Product Preview
SN74GTLPH1645	LVTTL/GTLP	16–bit LVTTL/GTLP high drive bus transceivers with ERC	56–pin TSSOP 56–pin TVSOP 56-ball VFBGA	Available
SN74GTLPH1655	LVTTL/GTLP	16–bit LVTTL/GTLP high drive universal bus transceivers with ERC	64–pin TSSOP	Available
SN74GTLPH3245	LVTTL/GTLP	32–bit LVTTL/GTLP high drive bus transceivers with ERC	114–pin LFBGA	Available
SN74GTLPH16612	LVTTL/GTLP	18–bit LVTTL/GTLP medium drive universal bus transceivers	56–pin SSOP 56–pin TSSOP	Available

26 VMEbus

The VMEbus is an asynchronous bus, which operates in a master/slave architecture. In 1987, the VMEbus specification was originally introduced as IEEE1014, but was altered several times to adjust to newer technologies and to increase the data throughput. New standards became the VME64, VME64x and finally the VME320 specification. VMEbus standards are governed by the VITA committee. TI was asked by the VITA committee to jointly develop a bus driver complying with the VME320 specification, but would be still backward compatible.

Table 28. Maximum Data Transfer Speeds

TOPOLOGY	BUS CYCLE PROTOCOL	MAXIMUM SPEED
VMEbus IEEE1014	BLT	40 Mbyte/sec
VME64	MBLT	80 Mbyte/sec
VME64x	2eVME	160 Mbyte/sec
VME320	2eSST	320 – 500+ Mbyte/sec

26.1 Electrical

The VMEbus uses push-pull totem pole outputs. For the VME320, LVTTL levels are used with a ±48-mA output drive. For the implementation of the VME320 bus a special star interconnection method is used to reach higher speeds.

26.2 Protocol

Depends on the VMEbus topology (see Table 28)

26.3 Applicability

The VMEbus is often used in a wide variety of applications. The main areas are still industrial, such as factory automation, and robotics; or in aerospace, e.g., fly-by-wire systems.

26.4 Features

- Live insertion capability
- Up to 21 slots in backplane
- Asynchronous data transfer
- Error detection
- Up to 64 address and data bits

Table 29. Top Device List VME

DEVICE	SPECIFICATION	DESCRIPTION	PACKAGE	STATUS
SN74VMEH22501	LVTTL	8-Bit Universal bus transceiver and two 1-bit bus transceivers with 3-state outputs up to 1 Gbyte/sec	48-pin TSSOP 48-pin TVSOP 56-ball VFBGA	Available

27 Stub Series Terminated Logic (SN74SSTLxxx)

Stub series terminated low-voltage logic designers are constantly trying to get the most out of their designs in the most cost-effective manner. As faster versions of a particular CPU become available, the designer often tries to improve the throughput of an existing design simply by increasing the CPU clock frequency.

These issues resulted in JEDEC defining two SSTL switching standards (SSTL_3, EIA/JESD8-8, and SSTL_2, EIA/JESD8-8). Both standards specify a particular termination scheme with appropriate values for the resistors and capacitors.

The stub series terminated logic (SSTL) interface standard is intended for high-speed memory interface applications and specifies switching characteristics such that operating frequencies up to 200 MHz are attainable. The primary application for SSTL devices is to interface with SDRAMs.

Two resistors in parallel are used to establish a voltage level such that differential voltage swings can be used, and two different resistor value configurations can be acceptable.

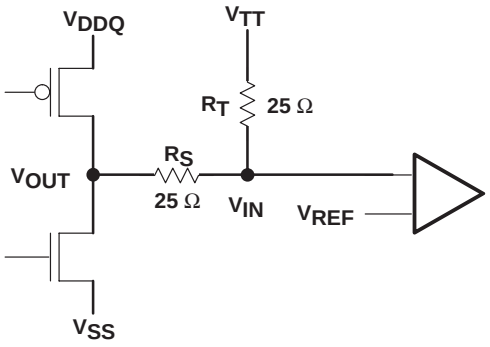


Figure 27. Typical Output Buffer Environment, Class II of SSTL Standard

Class I specifies an acceptable value of 50 Ω for the termination resistor R_T, and Class II specifies an acceptable value of 25 Ω. Figure 27 shows the typical dc environment for the output buffer (Class II); in this case an additional series resistor R_S is specified at 25 Ω. In order to meet the 400 mV minimum requirement for V_{IN}, a minimum of 8 mA must be driven into R_T, if R_T equals 50 Ω (Class I); or 16 mA if RT equals 25 Ω (Class II). The standard stipulates that for each value of R_T, a capacitive load equal to 10 pF or 30 pF can be used. The SSTL16837A supports both SSTL and LVTTL switching levels. Although the data sheet provides specifications where SSTL levels are used for the input and output levels, the device can operate under any combination of SSTL/LVTTL levels for the inputs and the outputs. When SSTL levels are applied to the device, it functions approximately 2 ns faster than when using LVTTL levels.

27.1 Electrical

The stub series terminated logic (SSTL) interface standard is intended for high-speed memory interface applications and specifies switching characteristics such that operating frequencies up to 200 MHz are attainable. The input high and low voltage levels (V_{IH} and V_{IL}) are V_{REF} + 200 mV and V_{REF} − 200 mV, resulting in a worst case noise margin of 25%. This seems to be a relatively small noise margin, but because it is a terminated bus, the actual noise source would have to be a fairly high current to produce 400 mV across the relatively low-impedance termination.

All totem-pole outputs of the SSTL compatible devices have a dedicated V_{DDQ} supply that (as stated in the SSTL_3 and SSTL_2 JEDEC standards) can be lower than or equal to V_{DD}, but never greater than V_{DD}. This feature allows for the internal circuitry supply voltage to be raised to 3.6 V for maximum speed performance, while lowering V_{DDQ} to prevent the device from dissipating large amounts of power in the output stage.

Irrespective of the input and output switching levels however, the characteristic high-level and low-level output drive current of 20 mA is maintained.

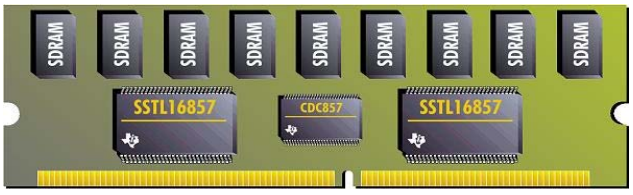
27.2 Protocol

Not specified.

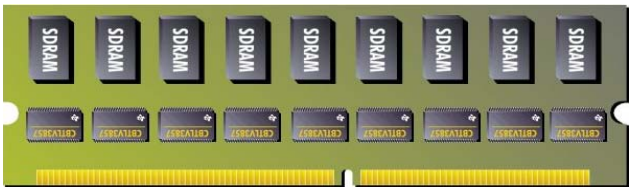
27.3 Applicability

Figure 28 shows a complete DDR SDRAM (SDRAM II) memory interfacing solution offered from Texas Instruments. Using a specially designed register, low-voltage bus switches, and a differential clock, DDR SDRAM modules can achieve double the memory data rate by allowing the SDRAMs to operate at twice their system frequency using the rising and the falling edge of the system clock.

The 14-bit registered buffer SSTL16857 is designed for 2.3-V to 3.6-V V_{CC} operation and differential data input and output levels. It buffers DDR SDRAM address and control signals. The CDC857 differential clock completes the TI solution for 184-pin DDR SDRAM modules. Optionally, the SSTL_2 optimized CBTLV3857 provides bus isolation in the DDR SDRAM DIMM application and reduces the capacitive loading on the data lines.



Front View



Back View

Figure 28. DDR SDRAM Memory Interfacing Solution Using the SN74SSTL16857

27.4 Features

- Maximum frequency of 200 MHz enables fast DDR SDRAM memory buses
- Supports both SSTL and LVTLL switching levels, which enables any combination of SSTL and LVTTL levels for inputs and outputs
- SSTL and LVTTL levels for inputs and outputs
- Outputs have dedicated V_{DDQ}, which can be lower or equal to V_{DD}. This enables the internal circuitry supply voltage to be raised to 3.6 V for maximum speed, while lowering V_{DDQ} to prevent the device from large power dissipation in the output stage.

Table 30. Top Device List for Stub Series Termination Logic

DEVICE	SPECIFICATION	DESCRIPTION	PACKAGE	STATUS
SN74SSTL16837A	SSTL_3	20-Bit SSTL_3 interface universal bus driver with 3-state outputs	64-pin TSSOP	Available
SN74SSTL16847	SSTL_3	20-Bit SSTL_3 interface buffer with 3-state outputs	64-pin TSSOP	Available
SN74SSTL16857	SSTL_2	14-Bit SSTL_2 registered buffer	48-pin TSSOP	Available
SN74SSTV16857	SSTL_2	14-Bit registered buffer with SSTL_2 inputs and outputs	48-pin TSSOP 48-pin TVSOP	Available
SN74SSTV16859	SSTL_2	13-Bit registered buffer with SSTL_2 inputs and outputs	48-pin TSSOP	Available
SN74SSTV32852	SSTL_2	24-Bit registered buffer with SSTL_2 inputs and outputs	114-ball LFBGA	Available
SN74SSTV32867	ULTTL	26-Bit registered buffer with SSTL_2 inputs and LVCMOS outputs	96-ball LFBGA	Available
SN74SSTV32877	SSTL_2	26-Bit registered buffer with SSTL_2 inputs and outputs	96-ball LFBGA	Available
SN74SSTVF16857	SSTL_2	14-Bit registered buffer with SSTL_2 inputs and outputs	48-pin TSSOP 48-pin TVSOP	Available

28 Clock Distribution Circuits (CDC)

Every digital system needs clock signals to synchronize the system activity. TI is developing new CDC products to meet the growing demand and high performance expectations of the communications, wireless infrastructure, optical networks, DIMM, and consumers markets.

To meet the stringent clock-signal timing requirements of today's system, a series of single-ended and differential clock buffers, low-jitter zero-delay buffers, clock synchronizer and jitter cleaner, Rambus clock generators, and synthesizers are available.

28.1 Electrical

This type of circuits has no industry standard except clock circuits for DIMM (SRAM, DDR and Rambus).

28.1.1 Clock Buffer/Driver

The clock distribution circuit receives one input clock and distributes the input clock to several clock outputs with the same frequency.

28.1.2 Zero Delay Buffer

Zero delay buffer is PLL-based circuitry whose input clock edge is in phase with the output clock edge so that the delay between input to output becomes almost zero.

28.1.3 Clock Synchronizer and Jitter Cleaner

Clock synchronizer and jitter cleaner are low phase noise and low skew clock circuits that synchronize a high-accuracy VCXO clock to a reference clock. Its output is a precise, and low-jitter clock.

28.1.4 Synthesizer

The PLL-based clock circuitry receives low frequency signals from the crystal or other source and delivers different frequency output signals according to system needs.

28.2 Protocol

No protocol is specified for CDC devices. This is dependent on applications. However, the following definition of some parameters are related to clock drivers.

Definitions of some basic parameters related to clocks:

Propagation Delay: Propagation delay is the time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high-to-low) to the other (low-to-high) defined level.

Output Skew: Output skew is the difference between the propagation delays of any two outputs of the same device at identical transitions.

Pulse skew: Pulse skew is the magnitude of the time difference between the high-to-low and the low-to-high propagation delays when a single switching input causes one or more outputs to switch.

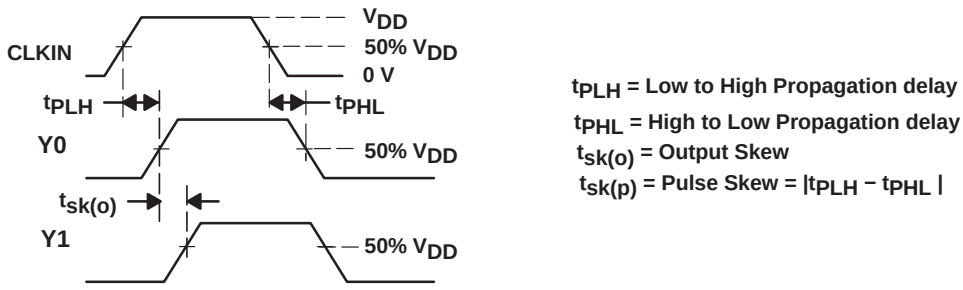


Figure 29. Input and Output Waveforms

Part-to-Part Skew: Part-to-part skew is defined as the magnitude of the difference in propagation delays between any specified outputs of two separate devices operating at identical conditions. The devices must have the same input signal, supply voltage, ambient temperature, package, load, environment, etc.

Static Phase Offset: Static phase offset is the time difference between the *averaged* input reference clock and the *averaged* feedback input signal when the PLL is in locked mode.

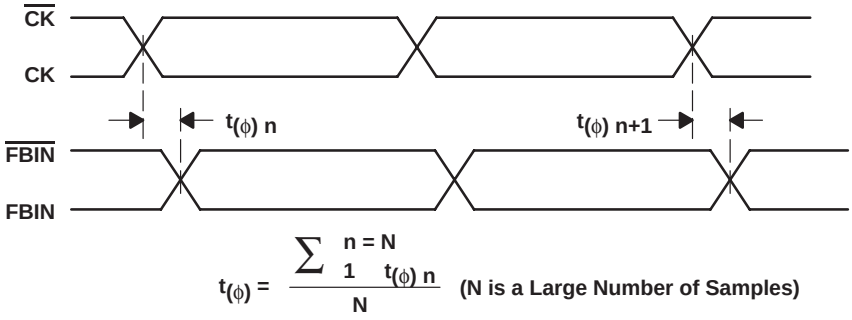


Figure 30. Static Phase Offset

Dynamic Phase Offset: Dynamic phase offset is the phase difference between input clock and feedback input clock due to the inability of the PLL to instantaneously update the feedback clock when the period of the input clock changes.

Jitter: Jitter is the dispersion of a time parameter of the pulse waves in a pulse train with respect to reference time, interval, or duration.

Peak-to-Peak Jitter: Peak-to-peak jitter is defined as the upper and lower bounds of a large number of samples of cycle-to-cycle period measurements from ideal.

Cycle-to-Cycle Jitter: Cycle-to-cycle jitter is the difference in the period of successive cycles of a continuous clock pulse train.

PLL Loop Bandwidth: PLL loop bandwidth is that region where the PLL is able to track phase and frequency modulation of the reference signal as long as the modulation frequencies remain as an angular frequency band roughly between zero and the natural frequency of the PLL.

Spread Spectrum Clock (SSC) Compatible: A PLL clock driver is SSC compatible if the PLL is able to track the modulation profile, and frequency is minimum tracking skew.

28.3 Applicability

28.3.1 Clocks Drivers for TI Serdes

All serializer-deserializers (serdes) require a low jitter clock to perform its operation correctly. Since the input duty cycle and jitter are very critical to serdes operation, TI clocks are readily available to meet these requirements. The peak-peak jitter requirement for the TLK1201, TLK1501, TLK2201, TLK2501, TLK2701, TLK2711, and TLK3101 is less than 40 ps; and CDCV304 is an excellent clock driver for these serdes, adding just 20 ps peak-peak jitter, on average.

The RMS jitter requirement of SLK2501, and SLK3104 is less than 3 ps. The CDCVF111 and CDC111 add very negligible jitter to its output. This differential clock driver has nine outputs and very low output skew.

Table 31. Recommended Clock Drivers for Serial/Gigabit Transceivers

SERIAL/GIGABIT TRANSCEIVER	RECOMMENDED CLOCK DRIVER
SLK2501	CDCVF111, up to 622.08 MHz CDC111, up to 500 MHz
TLK3104SC	CDCVF111, up to 622.08 MHz CDC111, up to 500 MHz
TLK3114SA	CDC111/CDCVF111
TLK1201, TLK1501, TLK2201, TNETE2201B, TLK2501, TLK2701, TLK2711, TLK3101	CDCV304, up to 140 MHz

28.4 Memory Clock Driver

TI offers PLL clock drivers for PC100/133, and double data rate (DDR) memory. These clock drivers are JEDEC-standard compliant. For robust design and advanced process, these PLLs are widely used in the buffered DIMM module.

Table 32. Clock Drivers for Memory Module

CLOCK DRIVER	APPLICATION SPACE
CDCVF2510, CDCVF2509	PC100/133
CDCV857, CDCV857A, CDCV857B, CDCU877	DDR

28.5 High-Speed LVDS/LVPECL/LVTTL Clock Buffers

The communication and ONET world need very low jitter high-speed clock buffers. A precise clock is the backbone of the whole operation. TI offers many high-speed differential clocks especially suitable for this space.

DEVICE NAME	DESCRIPTIONS
CDCVF111/CDC111	1:9 Differential PECL clock buffer
CDCLVP110	2:10 PECL High frequency clock driver
CDCLVD110	2:10 LVDS clock driver
CDCVF2310	1:10 LVTTL clock buffer

28.6 Adjusting Input to Output Delay

The phase-locked loop (PLL) clock drivers can adjust the input-to-output delay by simply changing feedback length, or feedback and load capacitance. The PLLs make the input-to-output delay zero by comparing the feedback signal with input signal, but the PLLs also can advance the output edge with respect to input edge.

DEVICE NAME	DESCRIPTIONS
CDCVF2505	1:5 PLL clock driver
CDCVF25081	1:8 PLL clock driver
CDCV855	1:5 Differential PLL clock driver
CDCV850	1:10 Differential PLL clock driver

28.7 Jitter Cleaner

In communications and many other applications, low-jitter clock is the most critical requirement. An effective way to ensure low-jitter is to use a phase-locked loop (PLL) clock with low loop bandwidth to filter the noise of the reference clock.

DEVICE NAME	DESCRIPTIONS
CDC5801	Low cost jitter cleaner
CDC7101	All digital PLL multiplier/divider with jitter cleanup
CDC7005	High performance clock synthesizer with selectable loop bandwidth

28.8 Multipliers and Dividers

TI offers a number of clock-multiplying and dividing circuits. The PLL-based multiplier and divider have very low jitter and output skew.

DEVICE NAME	DESCRIPTIONS
CDC5801	4x, 6x, 8x and 1/2x, 1/3x, 1/4x clock multiplier and divider
CDC536, CDC2536, CDC582, CDC2582, CDC586, CDC2586	1x, 1/2x and 2x option
CDCVF25084	4x multiplier

29 Summary

This *Comparing Bus Solutions* application report shows that Texas Instruments provides a vast portfolio of data transmission products covering most of the commonly used communication standards. The offering ranges from typical backplane logic families like ABT, LVT and GTLP to more advanced serial transmission families like LVDS and IEEE1394, while still providing solutions for the mature TIA/EIA (formerly RS) standards such as 232 and 485.

By referring to this application report, choosing the correct standard and therefore the appropriate family, has been made easier. Simply by selecting the type of transmission, e.g., serial or parallel, the distance and the data rate, a designer can very quickly find what is needed and has an introduction to the family contained in the report, with Internet pages waiting to be browsed for additional information.

Texas Instruments is committed to maintaining a leadership position in the field of data transmission, and TI continues to increase the range of advanced products available to engineers.

30 References

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2. EIA/TIA-485, ISO/IEC 8482: Information Technology—Telecommunications and information exchange between systems—Twisted pair multi-point interconnections
3. CAN, ISO 11898, Controller Area Network
4. ISO/IEC 9316, Information Technology, Small Computer System Interface–2
5. EIA/TIA-232-E, ITU–T V.28
6. TIA/EIA-644, Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits
7. TIA/EIA-899, Electrical Characteristics of Multipoint-Low Voltage Differential Signaling (M-LVDS) Interface Circuits for Multipoint Data Interchange EIA/JESD8–A, Interface Standard for Nominal 3 V/3.3 V Supply Digital Integrated Circuits
8. EIA/JESD8–3, Gunning Transceiver Logic (GTL), Low-Level, High-Speed Interface Standard for Digital Integrated Circuits
9. IEEE1394–1995, High Performance Serial Bus
10. IEEE P896.1, Futurebus+ Logic Layer Specifications
11. IEEE P896.2, Futurebus+ Physical Layer and Profile Specifications
12. EIA/JESD8–8, Stub Series Terminated Logic for 3.3 V (SSTL_3)
13. EIA/JESD8–9, Stub Series Terminated Logic for 2.5 V (SSTL_2)
14. IEEE802.3z Gigabit Task Force
15. GMII Gigabit Media Independent Interface
16. USB Universal Serial Bus Specification Revision 1.1 (Compaq, Intel, Microsoft, NEC)

31 Glossary

ABT	Advanced BiCMOS technology, 5-V logic family with TTL-compatible input and output specification
ABTE	Enhanced transceiver logic. 5-V logic with reduced noise margins to achieve higher speeds on the backplane, TTL-compatible
Arbitration	The process by which nodes compete for ownership of the bus. The cable environment uses a hierarchical point-to-point algorithm, while the backplane environment uses the bit-serial process of transmitting an arbitration sequence. At the completion of an arbitration contest, only one node is able to transmit a data packet.
BTL	Backplane transceiver logic. Typical applications are parallel backplanes
BPS	Bits per second
CAN	Controller area network, a Field Bus Standard (ISO 11898), intended for industrial and automotive applications.
DCE	Data Communication Equipment
DDR SDRAM	Double data rate synchronous dynamic random access memory
Downstream	The direction of data flow from the host or away from the host. A downstream port is the port on a hub electrically farthest from the host that generates downstream data traffic from the hub. Downstream ports receive upstream data traffic.
DTE	Data Terminal Equipment
EMI	Electromagnetic interference
Endpoint	An endpoint is capable of consuming an isochronous data stream that is sent by the host.
GTL	Gunning transceiver logic. GTL+ and GTLP are derivatives of GTL that operate at enhanced noise margin signal levels (V_{TT} = 1.5 V, V_{REF} = 1 V and V_{OL} = 0.55 V). GTLP is normally associated with optimized edge rate devices that allow high frequency operation in heavily loaded backplane applications.
Hub	A USB device that provides additional connections to the USB. Typical applications are parallel backplanes
HVD	High voltage differential

Isochronous	The term isochronous indicates the essential characteristic of a time scale or a signal such that the time intervals between consecutive significant instances either have the same duration or multiples of the shortest duration.
Live Insertion/Removal	The ability to attach and remove devices while the system is in operation
Link layer	The layer, in a stack of three protocol layers defined for the serial bus, which provides the service to the transaction layer of one–way data transfer with confirmation of reception. The link layer also provides addressing, data checking, and data framing. The link layer also provides an isochronous data transfer service directly to the application.
LVD	Low voltage differential
LVDM	Low voltage differential signaling for multipoint applications
LVDS	Low voltage differential signaling as defined in TIA/EIA-644-A
LVTTL	Low voltage transistor-transistor-logic
M-LVDS	Multipoint – low voltage differential signaling, TIA/EIA-899, adding multipoint capabilities to LVDS-like signaling
Node	An addressable device attached to the serial bus with at least the minimum set of control registers. Changing the control registers on one node does not affect the state of control registers on another node.
NRZI	Nonreturn to zero invert. A method of encoding serial data in which ones and zeroes are represented by opposite and alternating high and low voltages where there is no return to zero (reference) voltage between encoded bits. Eliminates the need for clock pulses.
Packet (1394)	A serial stream of clocked data bits. A packet is normally the PDU for the link layer, although the cable physical layer can also generate and receive special short packets for management purposes.
Packet (USB)	A bundle of data organized in a group for transmission. Packets typically contain three elements: control information (e.g., source, destination, and length), the data to be transferred, and error detection and correction bits.

Physical layer	The layer, in a stack of three protocol layers defined for the serial bus, which translates the logical symbols used by the link layer into electrical signals on the different serial bus media. The physical layer ensures that only one node at a time is sending data and defines the mechanical interface for the serial bus. There is a different physical layer for the backplane and for the cable environment.
Pipe	A logical abstraction representing the association between an endpoint of a device and software on the host. A pipe has several attributes; for example, a pipe may transfer data as streams (stream pipe) or messages (message pipe).
PLL	Phase-locked loop: The PLL is a feedback circuit. The purpose of this circuit is to minimize phase error between the input signal and the output signal of the PLL. In the locked state, the PLL regulates continuously the phase between the f_{in} and f_{out}, maintaining the defined phase difference between both frequencies.
Port	A physical layer entity in a node that connects to either a cable or backplane and provides one end of a physical connection with another node.
RS	Recommended standard
SCSI	Small computer systems interface
SSTL	Series stub termination logic
Stubs	Short traces, branching from the backplane. Often found on memory modules.
Termination resistor	The termination resistor is used at the end of a line in order to avoid reflections of the transmitted signal. If the termination resistor is chosen equally to the line impedance the line is optimally terminated.
Transaction	The delivery of service to an endpoint; consists of a token packet, optional data packet, and optional handshake packet. Specific packets are allowed/required based on the transaction type.
Transfer	One of the four USB transfer types. Isochronous transfers are used when working with isochronous data. Isochronous transfers provide periodic, continuous communication between host and device.
Quadlet	Four bytes of data.

USB	Universal serial bus
Upstream	The direction of data flow towards the host. An upstream port is the port on a device electrically closest to the host that generates upstream data traffic from the hub. Upstream ports receive downstream data traffic.

32 TI Contact Numbers

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